EK-MS11P-TM-001

MS11-P MOS Memory

Technical Manual

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CHARACTERISTICS AND SPECIFICATIONS

1.1 INTRODUCTION

The MS11-PB (M8743-BA) is a metal oxide semiconductor (MOS), random access memory (RAM), which provides 512K X 16 bits of data storage. The MS11-PB is designed for use with the PDP-11 extended UNIBUS. (This memory is four times larger than the UNIBUS address space.) The memory is a slave device to the PDP-11 processor, or to any peripheral device designated bus master. The MS11-P protects its data with error correction code (ECC) bits, which increase memory reliability.

1.2 GENERAL DESCRIPTION

The MS11-P consists of a single hex-height module (M8743-BA) which contains the extended UNIBUS interface, timing and control logic, error correcting code (ECC) logic, and a MOS storage array. The module also contains circuitry for ECC initialization and memory refresh, and a control and status register (CSR).

You can set the memory starting address at any 8K boundary within the 2048K extended UNIBUS address space. (The extended UNIBUS contains 22 address lines as opposed to 18 UNIBUS address lines.) The MS11-P reserves the top 128K of the extended UNIBUS address space for the I/O peripheral page.

The MOS storage array is configured in 22-bit words, which consist of a 16-bit PDP-11 word and six check bits generated by the ECC logic. The error correction code allows the MS11-P to detect a single-bit or double-bit error within the 22-bit word, and to correct a single-bit data error. The MS11-P does not correct a double-bit error, but can be configured to cause a parity error trap on a double-bit error. A single-bit error is transparent to the extended UNIBUS.

The memory storage elements are 65536 X 1 bit, MOS dynamic RAM devices. The MOS storage array contains 22 of these devices for each 64K bank of PDP-11 memory. Therefore, a memory module contains 176 storage devices. The MS11-P executes specially timed refresh cycles that periodically refresh the MOS storage devices. This ensures that data and check bits remain valid.

MOS storage devices are volatile (data is not retained when power is lost), so DIGITAL provides an optional battery backup unit to support the MOS power supply regulator(s). Therefore, during an ac power failure, dc power is available to MOS memory for a limited time only. The MS11-P memory module has inputs for two sources of +5 V power. These inputs are designated +5 VBB and +5 V. The +5 VBB module input is battery supported during an ac power failure; the +5 V input is not battery supported. The power distribution lines on the module are arranged to accommodate use of the battery backup option. In battery support mode, power is used only to refresh the MOS storage array so that battery backup time, and therefore data retention time, is maximized. A green LED on the module stays on as long as power is applied to the +5 VBB input.

If +5 VBB (and therefore data) is lost during an ac power failure, the MS11-P performs an error correction initialize (ECC INIT) operation after the power-up. For an ECC INIT operation, logical Øs and the corresponding check bit pattern are written into all 22-bit word locations in the MOS storage array. Signal AC LO is asserted by memory while ECC INIT is in progress.

The control and status register (CSR) in the MS11-P allows program control of certain ECC functions, and stores diagnostic information if an error has occurred. The CSR has its own address in the I/O peripheral page, and can be read or written into by any device designated as bus master.

Although the MOS storage array is configured in 22-bit words, the bus master sees the MS11-P as a standard 16-bit memory. The following paragraphs describe the memory response to the four types of data transfers (DATI, DATIP, DATO, and DATOB).

1.2.1 DATI or DATIP Data Transfer

Memory responds to a DATI or DATIP data transfer by performing a read cycle. (Memory interprets a DATIP data transfer as a DATI.) Memory retrieves the 22-bit word, that contains the requested data, from the MOS storage array, and calculates 6 check bits based on the 16 retrieved data bits. Then, memory compares the newly calculated check bits to the six retrieved check bits, which creates six syndrome bits. A logical 1 in the syndrome bit pattern indicates an error in the 22-bit word; an odd number of logical 1s indicates a single-bit error, while an even number of logical 1s indicates a double-bit error. If no error is detected, memory places the requested 16-bit data on the extended UNIBUS, and asserts the SSYN signal.

If a single-bit error is detected during a read cycle, the MS11-P initiates the following action.

1. A single-bit error within the 16 data bits is corrected.

2. Bit 4 in the CSR is set to 1.

3. A partial address of the requested data is recorded in the CSR, if CSR bit 15 is cleared to Ø.

4. The syndrome bits are logged in the CSR.

5. The requested 16-bit data and the SSYN signal are asserted on the extended UNIBUS after approximately a 230 ns delay. Therefore, the memory access time is increased due to a single-bit error.

Note that the syndrome bits determine if the single-bit error is contained in the retrieved data or check bits, and isolate a bad data bit. A check bit error is not corrected; however, the other single-bit error reactions are the same.

If a double-bit error is detected it is not corrected. However, the memory initiates the following actions.

1. Bit 15 in the CSR is set to 1.

2. A red LED on the module turns on, which indicates a double-bit (uncorrectable) error.

3. A partial address of requested data, pointing to a 1K block of memory, is recorded in the CSR. Any address information that relates to a previous error is destroyed. No future single bit error can record address information until the CSR is cleared.

4. The syndrome bits are logged in the CSR.

5. If bit zero in the CSR is set, the memory asserts BUS PBL which warns the processor that a double-bit (uncorrectable) error has occurred.

6. The requested 16-bit data and the SSYN signal are asserted on the extended UNIBUS after approximately a 230 ns delay. Therefore, the memory access time is increased due to a double-bit error.

1.2.2 DATO Data Transfer

Memory responds to a DATO data transfer by performing a write cycle. The data supplied by the bus master is latched-in from the extended UNIBUS. Memory calculates six checks bits, and then writes all 22 bits into the specified location.

1.2.3 DATOB Data Transfer

Memory responds to a DATOB data transfer by performing an internal read modify write (RMW) cycle. During the first portion of the RMW cycle, the data byte supplied by the bus master is latched-in from the extended UNIBUS, and the SSYN signal is asserted. The 22-bit word, which includes the specified byte, is then retrieved from the MOS storage array. Based on the 16 retrieved data bits, memory calculates 6 check bits and then compares them to the retrieved check bits, which creates 6 syndrome bits. The syndrome bits are examined to determine if the 22-bit word contains a single-bit or double-bit error. A single-bit error in the data is corrected, but a double-bit error in the 22-bit word is not corrected.

Data manipulation during the remainder of the RMW cycle is the same for a no error or corrected error condition. The 22-bit word is modified by merging the data byte supplied by the bus master, with the old data bytes from the storage array. Check bits are generated based on both data bytes, and the modified 22-bit word is then written into the MOS storage array.

If a double-bit error is detected during the first part of the RMW cycle, the old data and the old check bits are rewritten into the MOS storage array. Therefore, the double-bit error is preserved and will be flagged if the 22-bit word is retrieved during a DATI or DATIP data transfer. The data supplied by the bus master is lost.

1.3 SPECIFICATIONS

The following paragraphs contain MS11-P MOS memory specifications.

1.3.1 Functional Specifications

Capacity MS11-PB 524288 (512K)	16-bit PDP-11 words
Refresh timing Cycle time	675 ns (typical), 725 ns (maximum)
Repetition rate	One cycle every: 13.3 u (typical) 11.25 u (fastest) 13.75 u (slowest)

NOTE

Refresh cycle time is the time interval between the assertion of REF REQ L and the negation of BUSY L. These signals are internal to the memory module.

ECC INIT time 950 ms (maximum)

NOTE

ECC INIT time is the time interval between the negation of DC LO (at the memory receiver output) and the negation of AC LO (on the extended UNIBUS) by memory.

Access and Cycle times (Table 1-1)

NOTE

Access time is the time interval between memory reception of MSYN (at the bus receiver's input) and the assertion of SSYN on the UNIBUS.

Cycle time is the interval between memory reception of MSYN (at the bus receiver's output) when memory is not busy, and the negation of BUSY L.

Table 1-1 Access and Cycle Times

Data Transfer		Access Time (ns) Typical	Access Time (ns) Maximum	Cycle Time (ns) Typical	Cycle Time (ns) Maximum
DATI/DATIP	(memory)	490 (720 w/err)	535 (750 w/err)	680	750
DATO	(memory)	100	125	580	620
DATOB	(memory)	--	--	1100	1150
DATI/DATIP	(CSR)	--	530	--	--
DATO	(CSR)	--	220	--	--

1.3.2 Electrical Specifications

Voltage requirements	+5 V +5%, maximum ripple = Ø.2 V peak-to-peak +5 VBB +5%, maximum ripple = Ø.2 V peak-to-peak
Current and power requirements	(Refer to Tables 1-2 and 1-3)

NOTE

The total module consumption of +5 V current during normal operation is equal to the sum of the +5 V and +5 VBB ratings.

Table 1-2 Current Requirements (Amps)

	Typical	Maximum
+5 V	3.4 A	4.8 A
+5 VBB Active	2.Ø A	2.8 A
+5 VBB Standby	1.7 A	2.4 A

Table 1-3 Total Module Power Requirements (Watts)

	Typical	Maximum
Active	27. W	38 W
Standby	25.5 W	36 W
Battery Backup	8.5 W	12 W

1.3.3 Physical and Environmental Specifications

Module designation	MS11-PB	M8743-BA
Hex-height multilayer	21.6 X 38.1 cm	(8.5 X 15 in)
Operating temperature	5° to 50° C (41° to 122° F)	
Humidity	10 to 95% (noncondensing)	

1.4 RELATED DOCUMENTS

You can find more reference information in the following documents.

Title	Document Number
MS11-P Field Maintenance Print Set	MP-01477
PDP-11 Peripherals Handbook	EB-05961
PDP-11/04/24/34a/44/70 Processor Handbook	EB-19402-20
PDP-11/44 System User's Guide	EK-11044-UG
PDP-11/44 System Technical Manual	EK-KD11Z-TM

You can order these documents from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

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For information about Microfiche Libraries, contact:

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CHAPTER 2
INSTALLATION AND PROGRAMMING

2.1 GENERAL

This chapter provides the information necessary to install and program the MS11-P. Installation procedures include switch/jumper settings, backplane placement, power voltage checks, and MAINDEC testing. Programming information includes a discussion of bit assignments in the control and status register (CSR).

2.2 INSTALLATION

Before you remove or replace an MS11-P memory module, exercise the following cautions.

CAUTION

Static charges can damage the MOS memory chips. Be careful how you handle the module and where you lay it down.

We recommend that you use an antistatic wrist strap when removing or replacing the MS11-P memory module. DIGITAL offers a wrist-strap kit, PN A2-M-Ø299-1Ø (Appendix A).

When you install or remove a memory module, make sure there is no dc voltage applied to the module.

If the green LED is on, the module is receiving +5 V from the power supply or battery backup. The power source must be off before you remove or replace a memory module.

2.2.1 Switch and Jumper Configurations

The MS11-P contains two switchpacks and five jumpers. One switchpack contains four switches (S1-1 through S1-4) and the other contains eight switches (S2-1 through S2-8). Figure 2-1 shows the switch and jumper locationsl. The switches specify the memory starting address and the CSR address. The jumpers are factory set and should not be changed in the field.

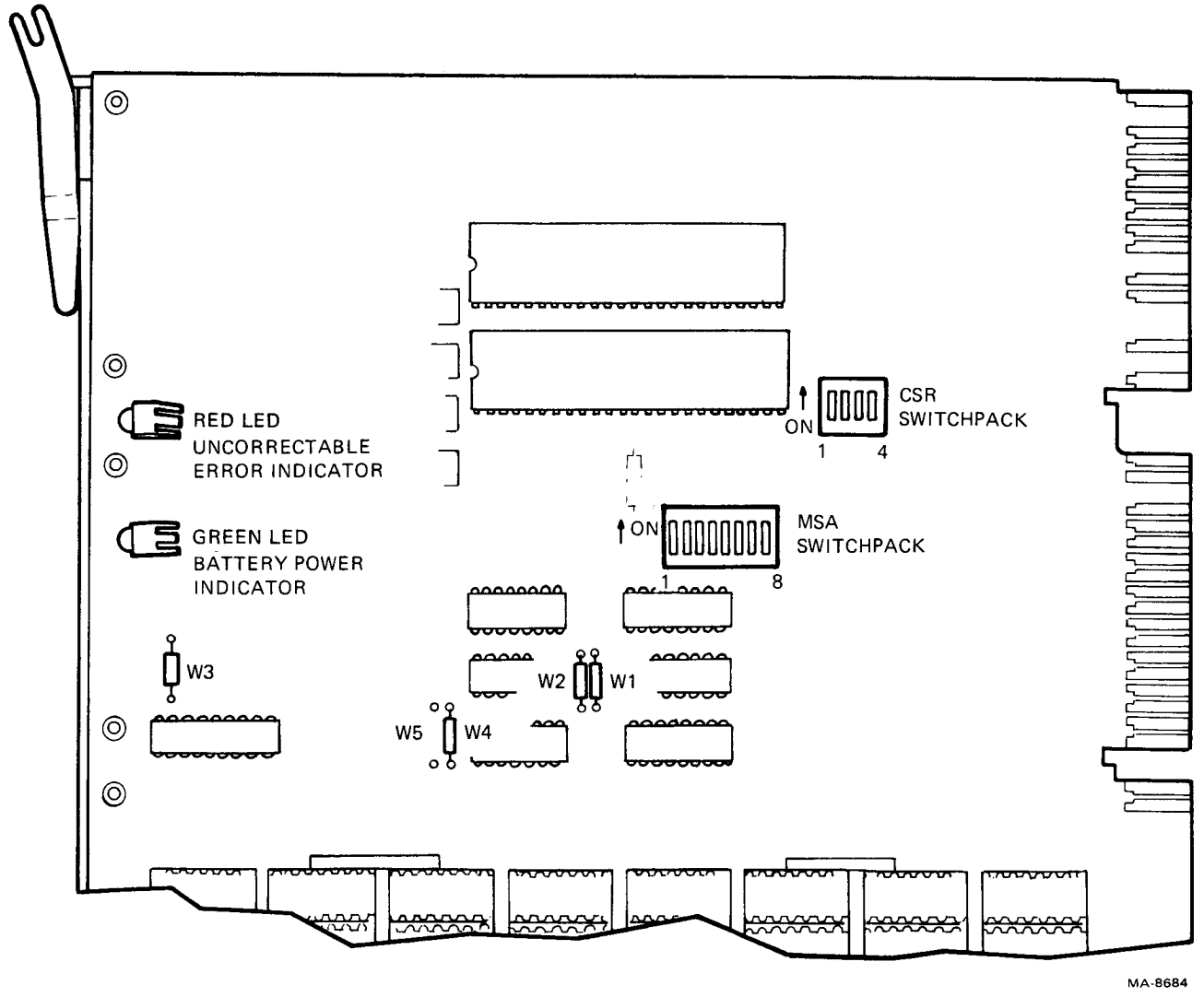


Figure 2-1 Switch and Jumper Locations

2.2.1.1 Memory Addressing -- PDP-11 Memory Conventions -- The MS11-P is designed for use with the PDP-11 extended UNIBUS (EUB). Memory in these computer systems provides storage for 16-bit data words, each of which contains two 8-bit bytes. These bytes are identified as low or high (Figure 2-2).

Each byte is addressable and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed by even numbered locations only, and the high (odd) byte for each word is automatically included.

Via the UNIBUS, 131,072 (128K) words or 262,144 (256K) bytes can be addressed. Via the extended UNIBUS, 2,097,152 (2048K) words or 4,194,034 (4096K) bytes can be addressed. A six-digit octal number specifies each byte location in UNIBUS memory. However, with the extended UNIBUS, an eight-digit octal number specifies each byte location. The address range is 000000--777777 on the UNIBUS and 00000000--17777777 on the extended UNIBUS (Figure 2-3).

Memory address decoding logic responds to the binary equivalent of the octal address. Figure 2-4 shows the binary equivalent of 00017772. The MS11-P decodes a 22-bit address (A21 -- A00) on the extended UNIBUS.

The memory starting address and storage capacity determine the address space on a bus occupied by a memory module. Switches on the MS11-P that correspond to address bits A21 -- A14 on the extended UNIBUS select a unique starting address. The block of addresses occupied by each module is continuous.

Memory Starting Address Selection -- The memory starting address (MSA) is the lowest bus address to which the MS11-P responds. You must assign the starting address to an 8K boundary within the 2048K extended UNIBUS address space. If you are adding memory to a system, find out how much memory the system has before you install the new memory module. That size is the added memory's starting address.

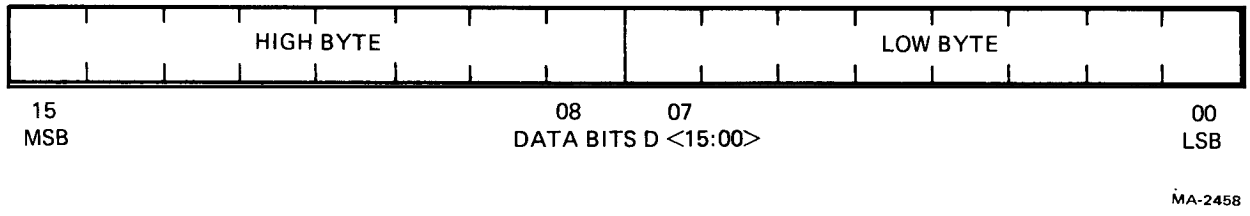


Figure 2-2 PDP-11 Data Word

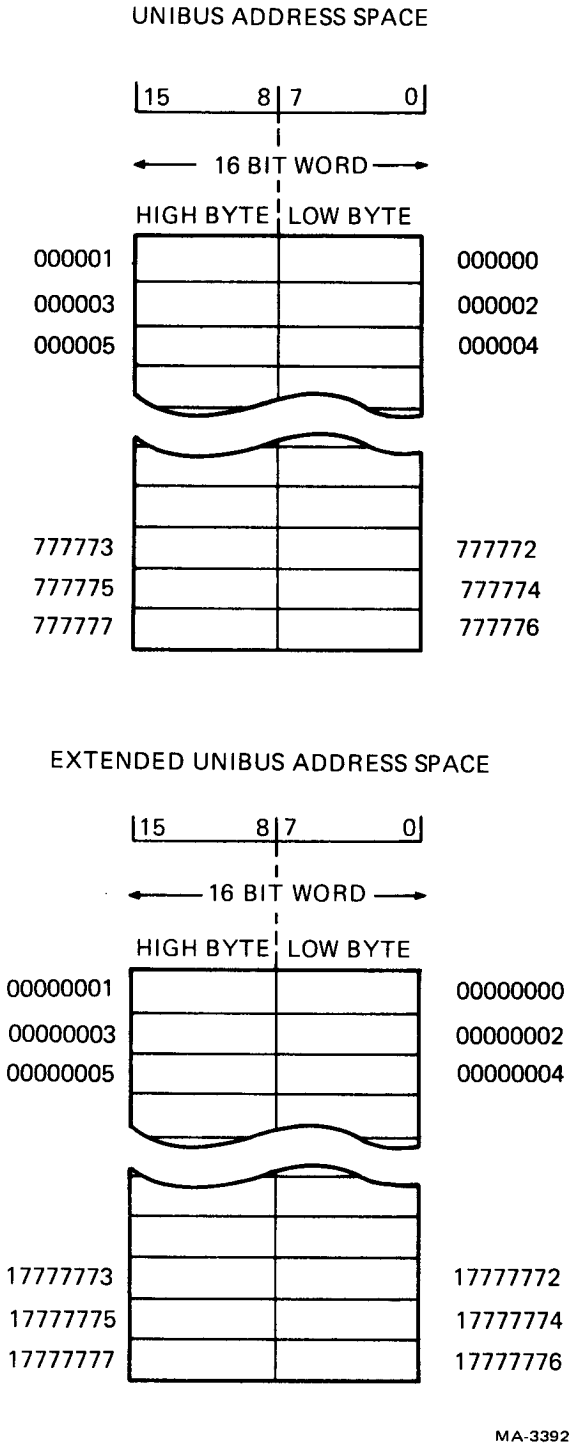


Figure 2-3 Bus Accessible Data Locations

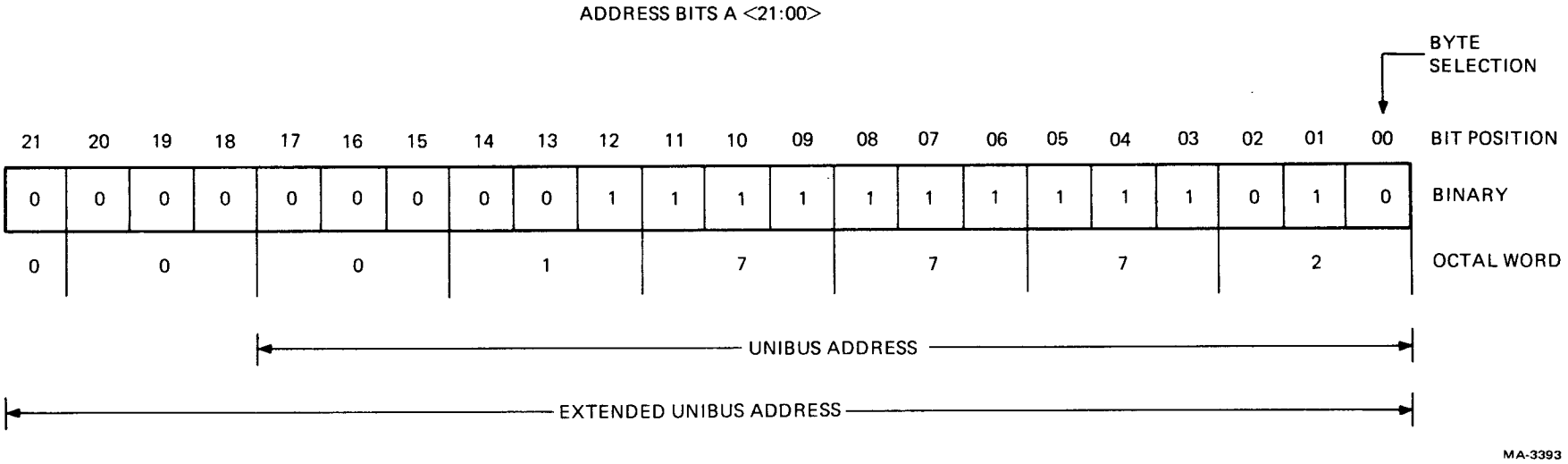


Figure 2-4 Octal and Binary Address

You assign the starting address by manually setting eight switches, S2-1 through S2-8, to the appropriate positions for the desired location. A switch in the off position corresponds to a logical one. Switches S2-1 through S2-3 correspond to address bits A21 -- A19 on the extended UNIBUS. Table 2-1 lists two groups of addresses. The first group of eight addresses is in increments of 256K decimal words which correspond to address bits A21 -- A19 (EUB). The second group of 32 addresses is in 8K decimal word increments which correspond to address bits A18 -- A14 (UNIBUS).

Determine the MSA switch settings for an MSA of 376K decimal words.

1. Find the 256K increment of the MSA.

   Table 2-1 lists the 256K increment as EUB address group 1. The switch column shows that S1 through S2 are closed and S3 is open.

2. Find the 8K increment of the MSA.

   Subtract the number in EUB group 1 (256K) from the MSA (376K). The result is 120K. Table 2-1 lists the 120K increment as UNIBUS group 15. The switch column shows that S4 is closed and S5 through S8 are open.

2.2.1.2 CSR Address Selection -- Address decoding logic in the MS11-P specifies the control and status register (CSR) address in the 17772100--17772136 range. Four switches, S1-1 through S1-4, select the CSR address. Switches S1-1 through S1-4 correspond to address bits A04 -- A01 respectively; a switch in the off position corresponds to a logical one. The CSR is always accessed as an entire data word, since bit A00 is not decoded by the CSR address logic.

The CSR address does not affect the MS11-P's memory starting address or storage capacity. However, it helps to assign CSR addresses to modules in the same order as the memory starting addresses. Each memory module's CSR is assigned a specific address. The memory module closest to the CPU is called module number 1. Table 2-2 shows that CSR switches selected for module one (CSR address 17772100) are all closed.

The next sequential CSR address is for memory module number 2 and so on, until CSR number 16 is reached. CSR 16 is the last reserved CSR address location.

Table 2-1 Starting Address Switches

EUB Group	Decimal K Words	Octal K Word	S1	S2	S3	S4	S5	S6	S7	S8
0	0000	0000 0000	C	C	C					
1	256	0200 0000	C	C	O					
2	512	0400 0000	C	O	C					
3	768	0600 0000	C	O	O					
4	1024	1000 0000	O	C	C					
5	1280	1200 0000	O	C	O					
6	1536	1400 0000	O	O	C					
7	1792	1600 0000	O	O	O					

UNIBUS Group	Decimal K Words	Octal K Word	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0000 0000				C	C	C	C	C
1	8	0004 0000				C	C	C	C	O
2	16	0010 0000				C	C	C	O	C
3	24	0014 0000				C	C	C	O	O
4	32	0020 0000				C	C	O	C	C
5	40	0024 0000				C	C	O	C	O
6	48	0030 0000				C	C	O	O	C
7	56	0034 0000				C	C	O	O	O
8	64	0040 0000				C	O	C	C	C
9	72	0044 0000				C	O	C	C	O
10	80	0050 0000				C	O	C	O	C
11	88	0054 0000				C	O	C	O	O
12	96	0060 0000				C	O	O	C	C
13	104	0064 0000				C	O	O	C	O
14	112	0064 0000				C	O	O	O	C
15	120	0074 0000				C	O	O	O	O
16	128	0100 0000				O	C	C	C	C
17	136	0104 0000				O	C	C	C	O
18	144	0110 0000				O	C	C	O	C
19	156	0114 0000				O	C	C	O	O
20	160	0120 0000				O	C	O	C	C
21	168	0124 0000				O	C	O	C	O
22	176	0130 0000				O	C	O	O	C
23	184	0134 0000				O	C	O	O	O
24	192	0140 0000				O	O	C	C	C
25	200	0144 0000				O	O	C	C	O
26	208	0150 0000				O	O	C	O	C
27	216	0154 0000				O	O	C	O	O
28	224	0160 0000				O	O	O	C	C
29	232	0164 0000				O	O	O	C	O
30	240	0170 0000				O	O	O	O	C
31	248	0174 0000				O	O	O	O	O

Table Switch Settings

C = closed (on)
O = open (off)

Table 2-2 CSR Switches

CSR Module Number	UNIBUS Address	LSB A1	A2	A3	MSB A4
1	17772100	C	C	C	C
2	17772102	O	C	C	C
3	17772104	C	O	C	C
4	17772106	O	O	C	C
5	17772110	C	C	O	C
6	17772112	O	C	O	C
7	17772114	C	O	O	C
8	17772116	O	O	O	C
9	17772120	C	C	C	O
10	17772122	O	C	C	O
11	17772124	C	O	C	O
12	17772126	O	O	C	O
13	17772130	C	C	O	O
14	17772132	O	C	O	O
15	17772134	C	O	O	O
16	17772136	O	O	O	O

Table Switch Settings

C = closed (on)
O = open (off)

2.2.2 Backplane Placement

The MS11-P is compatible with the PDP-11 extended UNIBUS (EUB), which is the main memory bus in the PDP-11/44.

When used with the PDP-11/44, the MS11-P should be inserted into any one of slots 9 through 12 in the processor backplane (PN 70-16502-00). Slots 9 through 12, sections A and B, contain the extended UNIBUS.

When used with the PDP-11/24, the MS11-P should be inserted into any one of slots 3 through 6 in the processor backplane. Slot 2 should hold the KT24 UNIBUS MAP option (M7134) to properly use the MS11-P capacity.

Table 2-3 shows the MS11-P backplane connections.

2.2.3 Power Voltage Check

Once primary power is on, you should check the following dc power voltages at the backplane.

Voltage and Tolerance	Backplane Pin
+5 V +5%	AA2, BA2, CA2
+5 VBB +5%	BB1, BD1

Table 2-3 MS11-P Pin Allocation (M8743)

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A	INIT L	+5V		+5V	NPG IN H	+5V		+5V		+5V		+5V
B		BOOT EN L	+5V BAT		NPG OUT H							
C	DØØ L	GND		GND		GND		GND		GND		GND
D	DØ2 L	DØ1 L	+5V BAT									
E	DØ4 L	DØ3 L	A19 L	A18 L								
F	DØ6 L	DØ5 L	AC LO L	DC LO L								
H	DØ8 L	DØ7 L	AØ1 L	AØØ L								
J	D1Ø L	DØ9 L	AØ3 L	AØ2 L								
K	D12 L	D11 L	AØ5 L	AØ4 L				BG7 SO H				
L	D14 L	D13 L	AØ7 L	AØ6 L				BG7 OUT H				

Table 2-3 MS11-P Pin Allocation (M8743) (Cont)

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
M		D15 L	AØ9 L	AØ8 L				BG6 SO H				
N	A21 L	PB L	A11 L	A1Ø L				BG6 OUT H				
P	A2Ø L		A13 L	A12 L				BG5 SO H				
R			A15 L	A14 L				BG5 OUT H				
S			A17 L	A16 L			INH REFL TP	BG4 SO H				
T	GND		GND	C1 L	GND		GND	BG4 OUT H	GND		GND	
U			SSYN L	CO L								
V			MSYN L									

Modified UNIBUS or EUB

NOTE: Pins marked by a bracket are tied together on the module to provide grant continuity.

2.2.4 MAINDEC Testing

You should use the MS11-L/M/P Memory Exerciser (MAINDEC-11-CZMSPA) diagnostic program with the MS11-P memory module. To check correct memory operation, follow the procedure described in Paragraph 2.2.4.1. No double errors are permitted. Also, make sure the program printout confirms the total memory in the system.

2.2.4.1 Test Procedure

Do the following steps to test correct memory operation.

1. Set the starting address and CSR address for each MS11-P according to Paragraph 2.2.1.

2. Run the CZMSPA diagnostic. (Refer to the printout example.) Run two passes. The first pass defaults to a quick verification (QV).

3. If four MS11-Ps are installed, follow the same procedure as above; but, after the diagnostic pass for all four modules, do the following extra steps.

   a. Remove the modules with the lowest and highest starting addresses. Reset the switch settings on the modules so their starting addresses are swapped. Reinstall the two modules in the backplane. Do this because the diagnostic cannot test the upper 128K of the highest address module, since this memory space is reserved for the I/O page.

   b. Start the diagnostic again and run one pass. Run the diagnostic until the lowest addressed module has been tested. One pass in the QV mode will take eight minutes.

4. All the diagnostic passes should be error-free.

Following these four steps helps you make sure all memory is installed successfully.

NOTE

Paragraph 4.3.6 is a simplified toggle-in memory test.

```
*** TEST DISPLAY PRINTOUT ***

>>>b dxØ

CHMDXB1 XXDP+ DX MONITOR
BOOTED VIA UNIT Ø
28K UNIBUS SYSTEM

ENTER DATE (DD-MMM-YY):

RESTART ADDR: 152Ø1Ø
THIS IS XXDP+.  TYPE "H" OR "H/L" FOR HELP.

r zmsp??

 CZMSPA MS11-L/M/P MEMORY DIAGNOSTIC
 11/44 CACHE AVAILABLE

CSR MAP

CSR Ø 1 2 3 4 5 6 7 8 9 A B C D E F

MEMTYPE P

512K OF MS11-P
512K WORDS OF MEMORY TOTAL

                    MEMORY CONFIGURATION MAP
                         16K WORD BANKS
         1       2       3       4       5       6       7
   Ø12345670123456701234567012345670123456701234567012345670123
ERRORS
INTRLV   --------------------------------
MEMTYPE  PPPPPPPPPPPPPPPPPPPPPPPPPPPPPP
CSR      ØØØØØØØØØØØØØØØØØØØØØØØØØØØØ
PROTECT PP
BANK= 1Ø  TEST=31
BANK= 13  TEST=33
BANK= 16  TEST=33   Optional display with CTRL/T
BANK= 21  TEST=24
BANK= 24  TEST=24
BANK= 3Ø  TEST=33
END PASS #QV 1
END PASS # 2
```

2.3 CSR BIT ASSIGNMENT

The control and status register (CSR) in the MS11-P allows program control of certain ECC functions, and contains diagnostic information if an error has occurred. The CSR has an assigned address and can be accessed by a bus master via the extended UNIBUS. The assertion of BUS INIT L clears some CSR bits. BUS INIT L is asserted for a short time after system power has come up, or in response to a reset instruction. Figure 2-5 shows the CSR bit assignments described in Paragraph 2.3.1 through 2.3.9. Note that all unused bits are read as zero. Paragraphs 2.3.10 and 2.3.11 give more detailed CSR usage information.

2.3.1 Uncorrectable Error Indication Enable (Bit 0)

If a double error occurs with ECC enabled, or a single or double error occurs with ECC disabled and bit 0 set, then during a DATI or DATIP cycle to memory, BUS PB L is asserted on the UNIBUS at the same time as data.

This is a read/write bit reset to zero on power up or BUS INIT.

2.3.2 Disable Correction Mode (Bit 1)

This bit is a diagnostic aid which allows reading data from memory without interference from error correction circuitry. When bit 1 is set, no single errors are corrected. A single error sets CSR bit 4 and CSR bit 15, and a double error sets CSR bit 15.

This is a read/write bit reset to zero on power up or BUS INIT.

2.3.3 Diagnostic Check Mode (Bit 2)

This bit is a diagnostic aid which allows reading or writing the check bits at a given memory location. Bit 2 also allows reading the error syndromes after a single or double error.

Example 1 shows how to write check bits to a memory location.

Example 1

- Write the desired check bits into CSR bits 5 through 10, and enable diagnostic check mode.
- A subsequent DATO or DATOB to memory writes the check bits stored in CSR bits 5 through 10 to the check bit RAMs.

Example 2 shows how to examine the check bits at a memory location.

Example 2

- Write the CSR to enable diagnostic check mode.
- A subsequent DATI or DATIP to memory reads the check bits stored in memory and clocks them into CSR bits 5 through 10. The check bits can then be examined by reading the CSR.

15	Uncorrectable error							
14	EUB error							
	Address retrieval							
13	Set inhibit mode							
12	Reserved (always read as zero)							
11	A17		Ø		1 if bits 2, 13, 14 = 1			
10	A16		Ø		Ck bit 8		Syn bit 8	
9	A15	Error address	Ø	Error address	Ck bit 4	Diag chk mode only	Syn bit 4	Loaded only when
8	A14	Read when	A21	Read when	Ck bit 2	CSRØ2=1 and after	Syn bit 2	there is a single
7	A13	CSR14=Ø or	A20	CSR14=1 or	Ck bit 1	memory read or	Syn bit 1	or double error and
6	A12	CSR15=1 or	A19	CSR15=1 or	Ck bit Ø	after CSR	Syn bit Ø	CSR2=Ø/ read only
5	A11	CSR14=Ø CSRØ4=1	A18	CSR14=1 CSRØ4=1	Ck bit X	write with CSRØ2=1	Syn bit X	when CSRØ2=1
4	Single error							
3	Inhibit mode pointer		Ø protects 1st 16K 1 protects 2nd 16K			Used with CSR 13		
2	Diagnostic check							
1	Disable correction mode							
Ø	Uncorrectable error indication enable							

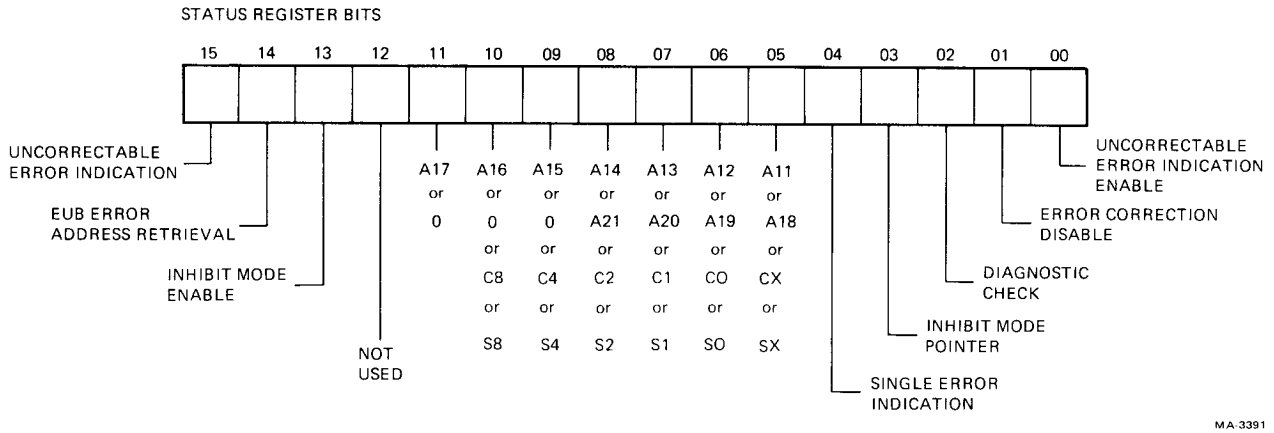


Figure 2-5 CSR Bit Allocation

If a single or double error occurs during normal memory operation, the SERR or DERR bit respectively in the CSR is set, and the error syndrome bits and error address bits are stored in CSR bits 5 through 11. In diagnostic check mode, the error syndrome bits are read when CSR bits 10 through 5 are read.

This bit is a read/write bit reset on power up or BUS INIT.

2.3.4 Inhibit Mode Pointer (Bit 3)

This bit works in conjunction with set inhibit mode (bit 13). When bit 13 is set to 1, a 16K portion of memory is inhibited from operating in disable correction mode or diagnostic check mode.

The inhibit mode pointer indicates which 16K is being inhibited. For example, if bit 3 equals 0, the first 16K of memory is inhibited, and if bit 3 equals 1, the second 16K of memory is inhibited.

If bit 13 is set to 0, this bit has no effect.

Therefore bit 3, in conjunction with bit 13, allows a 16K portion of memory to always have ECC coverage. The systems diagnostic can reside in this protected portion of memory and disable error correction, and/or run diagnostic check mode in the rest of memory without itself becoming vulnerable to single errors.

This bit is a read/write bit reset by power up and BUS INIT.

2.3.5 Single Error (Bit 4)

If a single bit error is detected on a DATI or DATIP cycle, bit 4 is set.

During normal operation, when a single bit error is detected, the error address and syndromes are logged in CSR bits 5 through 11 (unless uncorrectable error CSR bit 15 is set). The error address and syndromes are logged unconditionally in the disable correction mode.

If a single bit error is detected on a DATI or DATIP cycle to memory while in DIAG CHECK mode, CSR bit 4 is set, but the error address and syndromes are not logged in the CSR.

This bit is a read/write bit reset by power up or BUS INIT.

2.3.6 Error Address and Check Bit Storage (Bits 5 -- 11)

2.3.6.1 Check Bit Storage (Diagnostic Check Bit 2 = 1, Disable Correction Bit 1 = Do Not Care) -- These bits are read/write bits in diagnostic check mode. They store the check bits to be written into, or read from, memory.

A one is read in CSR bit 11 if CSR bits 2, 13, and 14 are set to indicate that the memory under test is an MS11-P.

2.3.6.2 UNIBUS Address Storage (Diagnostic Check Bit 2 = Ø, Disable Correction Bit 1 = Do Not Care) -- These bits store address bits A11 through A17 if a double or single error occurs on a DATI or DATIP cycle.

2.3.6.3 EUB Address Storage (Diagnostic Check Bit 2 = Ø, Disable Correction Bit 1 = Do Not Care) -- If a double or single error occurs on a DATI or DATIP cycle, address bits A17 through A11 are stored in CSR bits 11 through 5, and address bits A21 through A18 are stored in a backup register. The EUB error address retrieval bit (CSR bit 14) is used to obtain the total error address as follows.

When CSR bit 14 equals Ø, a read to the CSR obtains A17 through A11 from CSR bits 11 through 5.

CSR bit 14 is now written to a one, and a read to the CSR then reads A21 through A18 from CSR bits 8 through 5, and zeros from CSR bits 11 through 9.

Address bits A21 through A11 are therefore obtained to locate the double error to a 1K portion of memory.

The EUB address A21 through A18 is read only when CSR 14 equals 1.

2.3.6.4 Syndrome Storage -- If, during normal operation, a double or single error occurs during a DATI, DATIP, or DATOB cycle, and if CSR bit 2 is set to Ø, CSR bits 5 through 1Ø store syndrome bits X, Ø, 1, 2, 4, and 8. To read syndrome bits from the CSR, CSR bit 2 must be set to 1 (diagnostic mode) and the CSR read. This operation allows syndrome bits for a single or double failure to be read, instead of the address bits normally read when CSR 2 is set to Ø.

2.3.7 Set Inhibit Mode (Bit 13)
When this bit is set to Ø, diagnostic check mode and/or disable correction mode can operate over the entire memory.

When this bit is set to 1, the inhibit mode pointer inhibits either the first or second 16K from going into diagnostic check or disable correction mode.

This bit is a read/write bit reset by power up or BUS INIT.

2.3.8 EUB Error Address Retrieval (Bit 14)
With bit 14 equal to Ø, a read to the CSR after an error fetches error address A17 through A11. With bit 14 equal to 1, a read to the CSR fetches address A21 through A18.

Setting bit 14 to 1 has the side effect of preventing memory from entering the diagnostic check mode.

This bit is a read/write bit reset on power up and BUS INIT.

2.3.9 Uncorrectable Error (Bit 15)

In normal operation or diagnotic check mode this bit is set on a DATI or DATIP when a double error is detected. Setting this bit also turns on a red LED on the board to indicate the error.

This bit is set in disable correction mode if a single or double error is detected.

This bit is a read/write bit reset on power up or BUS INIT.

2.3.10 Notes on CSR Usage

Bit 1 (error correction disable) is usually set to 1 for diagnostic purposes, which allows data to be read or written into memory without interference from the error correction logic. If bit 1 is set to 1, you can clear a soft double error in memory by writing new data into one or both PDP-11 memory locations of the bad 22-bit word. Note that a soft double error may be caused by one hard error and one soft error, or two soft errors, within a 22-bit word (a hard double error cannot be cleared).

Bit 2 (diagnostic check mode) allows check bits in the MOS storage array to be read via the CSR. Right after a DATI bus cycle to memory (with bit 2 equal to 1), the CSR should be read with a DATI cycle to examine the check bits retrieved from the storage array. Note that a DATO cycle to the CSR destroys the retrieved check bits, but an error address recorded in the CSR is preserved.

The diagnostic check mode also provides a way to test the error correction logic by allowing the check bit pattern in a 22-bit word to be altered via the CSR. The desired check bit pattern should be written into CSR bits 11 -- 5 and bit 2 should be set to 1 with a DATO cycle to the CSR. A DATO cycle to memory should then be performed. Writing the appropriate check bit pattern in the storage array should cause detection and correction of a single-bit error during a subsequent memory read cycle. (Refer to Paragraph 4.3.11, Diagnostic Check Mode Usage.)

If bit 13 is set to 1, bits 1 and 2 in the CSR do not affect the portion of memory specified by bit 3. The system diagnostic can reside in the protected portion of memory. The diagnostic can then disable error correction and/or run the diagnostic check mode on the rest of the memory module, without being vulnerable to single-bit errors itself.

With bit 15 or 4 set to 1 and bits 14 and 2 cleared to 0, you can retrieve the EUB error address (A21 -- A11) as follows.

1. Read the CSR with a DATI bus cycle to obtain A17 -- A11.
2. Write a logical 1 into CSR bit 14 with a DATO bus cycle.
3. Read the CSR with a DATI bus cycle to obtain A21 -- A18.

When the memory is not in diagnostic mode (CSR bit 2 equals 0), data previously loaded into CSR bits 11 -- 5 cannot be read.

2.3.11 More CSR Examples

The memory module does not inform the central processor unit (CPU) when a single error occurs. However, some operating systems poll the CSR periodically. If the operating system software sees that bit 4 is set, then it can perform a read to the CSR to read the address of the 1K block which contains the location of the 1-bit error. This address is bits A11 -- A17 in CSR bits 5 -- 11.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	A17	A16	A15	A14	A13	A12	A11	1	0	0	0	1

To read the higher order addresses, write bit 14 to a 1 (Xs are read only).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	X	X	X	X	X	X	X	0	0	0	0	1

Now read the CSR again. This reads address bits A21 -- A18 in CSR bits 8 -- 5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	A21	-	-	-	A18	0	0	0	0	1

To get the syndrome bits, set bit 2 to a 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	X	X	X	X	X	X	X	0	0	1	0	1

Now read the CSR. Error syndrome bits S8 -- SX are in CSR bits 5 -- 10.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	S8	S4	S2	S1	S0	SX	0	0	1	0	1

Now write CSR bit 2 to 0 to resume normal operation.

To load check bits into the CSR, write the desired check bits into CSR bits 10 -- 5 and enable diagnostic mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	C8	C4	C2	C1	C0	CX	0	0	1	0	0

Now, a write to a memory address takes these check bits from the CSR instead of from the EDC (error detection and correction circuit).

A read to a memory address takes the check bits stored in memory and loads them into bits 5 -- 10 in the CSR.

2.3.12 Summary Data Condition Tables

The following tables are summaries of the memory actions for each possible condition of data in each operating mode of memory.

Protected refers to the memory area when the module is in a diagnostic mode, but the data transaction is in the first or second 16K of memory, and unconditional protection of that area is enabled. Unprotected refers to any other area of memory.

Table 2-4 Read, No Errors

Normal operating mode	Data read from memory and placed on bus
Diagnostic mode /protected	Data read from memory and placed on bus like normal read cycle
Diagnostic mode /unprotected	Data read from memory and placed on bus like normal read cycle -- check bits read from memory are logged in CSR bits 5 -- 10
Disable correction mode /protected	Data read from memory and placed on bus like normal read cycle
Disable correction mode /unprotected	Data read from memory and placed on bus like normal read cycle
Diagnostic and disable correction mode /protected	Data read from memory and placed on bus like normal read cycle
Diagnostic and disable correction mode /unprotected	Data read from memory and placed on bus like normal read cycle -- check bits read from memory are logged in CSR bits 5 -- 10

Table 2-5 Read, Single Error

Normal operating mode	CSR 4 H is set. Data is corrected by EDC before it is placed on bus. If CSR 15 H is not set, A11 -- A21 and error syndrome bits are latched in CSR. If CSR 15 H was set on a previous DBE, but not cleared by software, there is no logging of the SBE so information from previous error can be read.
Diagnostic mode /protected	CSR 4 H is set. Data is corrected by EDC before it is placed on bus. Addresses and error syndromes are not logged in CSR.
Diagnostic mode /unprotected	CSR 4 H is set. Data is read from memory and corrected by EDC before it is placed on bus. Check bits read from memory are logged in CSR bits 5 -- 1Ø. No addresses or error syndrome bits are logged.
Disable correction mode /protected	CSR 4 H is not set. Data is corrected by EDC before it is placed on the bus. Addresses and error syndromes are not logged in CSR.
Disable correction mode /unprotected	CSR 15 H and CSR 4 H are set. With error correction disabled, a single bit error becomes an uncorrectable error. A11 -- A21 and error syndromes are logged in CSR. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data.
Diagnostic and disable correction mode /protected	CSR 4 H is set. Data is corrected by EDC before it is placed on bus. Addresses and error syndromes are not logged in CSR.
Diagnostic and disable correction mode /unprotected	CSR bits 4 and 15 are set. Data is read from memory and placed on bus. No correction takes place. Check bits read from memory are logged in CSR bits 5 -- 1Ø. Addresses and syndromes are not logged.

Table 2-6 Read, Double Error

Normal operating mode	CSR 15 H is set. All -- A21 and error syndromes are latched in CSR. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data.
Diagnostic mode /protected	CSR 15 H is set. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data. No other information is logged in CSR.
Diagnostic mode /unprotected	CSR 15 H is set. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data. Check bits read from memory are logged in CSR bits 5 -- 1Ø. No addresses or error syndromes are logged in CSR.
Disable correction mode /protected	CSR 15 H is set. All -- A21 and error syndromes are latched in CSR. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data.
Disable correction mode /unprotected	CSR 15 H is set. All -- A21 and error syndromes are latched in CSR. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data.
Diagnostic and disable correction mode /protected	CSR 15 H is set. Red LED turns on. If CSR Ø H is set, BUS PB L is asserted on bus at same time as uncorrected data. No other information is logged in CSR.
Diagnostic and disable correction mode /unprotected	CSR bit 15 is set. Data is read from memory and placed on bus. Check bits read from memory are logged in CSR bits 5 -- 1Ø. Addresses and syndromes are not logged.

Table 2-7 Write Cycle

Normal operating mode	Data is written to memory with check bits generated by EDC.
Diagnostic mode /protected	Data is written to memory with check bits generated by EDC. This is identical to write cycle in normal mode.
Diagnostic mode /unprotected	Data is written to memory with check bits that were loaded into CSR by diagnostic program instead of check bits from EDC.
Disable correction mode /protected	Data is written to memory with check bits generated by EDC. This is identical to write cycle in normal mode.
Disable correction mode /unprotected	Data is written to memory with check bits generated by EDC. This is identical to write cycle in normal mode.
Diagnostic and disable correction mode /protected	Data is written to memory with check bits generated by EDC. This is identical to write cycle in normal mode.
Diagnostic and disable correction mode /unprotected	Write cycles in this mode are treated like in diagnostic mode. Data is written to memory along with check bits that were loaded into CSR by diagnostic program instead of check bits from EDC.

Table 2-8 Byte Write, No Errors Detected During Read

Normal operating mode	New byte is combined with old byte and check bits are generated by EDC. Data and check bits are written to memory.
Diagnostic mode /protected	New byte is combined with old byte and check bits are generated by EDC. Data and check bits are written to memory.
Diagnostic mode /unprotected	New byte is combined with old byte. Data is written to memory along with check bits that were loaded into CSR by diagnostic program instead of check bits from EDC.
Disable correction mode /protected	New byte is combined with old byte and check bits are generated by EDC. Data and check bits are written to memory.
Disable correction mode /unprotected	New byte is combined with old byte and check bits are generated by EDC. Data and check bits are written to memory.
Diagnostic and disable correction mode /protected	New byte is combined with old byte and check bits are generated by EDC. Data and check bits are written to memory.
Diagnostic and disable correction mode /unprotected	Write cycles in this mode are treated like in diagnostic mode. New byte is combined with old byte. Data is written to memory along with check bits that were loaded into CSR by the diagnostic program instead of check bits from EDC.

Table 2-9 Byte Write, Single Error Detected During Read

Normal operating mode	CSR 4 H is set. All -- A21 and the error syndromes are logged in CSR (if CSR 15 H is not set). Bad data is corrected and combined with new byte. Check bits are generated by EDC on new 16-bit word. Data and check bits are written to memory.
Diagnostic mode /protected	CSR 4 H is set but addresses and syndromes are not logged in CSR. Bad data is corrected and combined with new byte. Check bits are generated by EDC on new 16-bit word. Data and check bits are written to memory.
Diagnostic mode /unprotected	CSR 4 H is not set and addresses and syndromes are not logged in CSR. Bad data is corrected and combined with new byte. Check bits are output from CSR. Data and check bits are written to memory.
Disable correction mode /protected	CSR 4 H is not set and addresses and syndromes are not logged in CSR. Bad data is corrected and combined with new byte. Check bits are generated by EDC on new 16-bit word. Data and check bits are written to memory.
Disable correction mode /unprotected	CSR 4 H and CSR 15 H are set. Addresses and syndromes are logged in CSR. Error is corrected and old byte is combined with new byte. Data is written to memory with check bits generated by EDC.
Diagnostic and disable correction mode /protected	CSR 4 H is set but addresses and syndromes are not logged in CSR. Bad data is corrected and combined with new byte. Check bits are generated by EDC on new 16-bit word. Data and check bits are written to memory.
Diagnostic and disable correction mode /unprotected	CSR 4 H is not set and addresses and syndromes are not logged in CSR. Bad data is corrected and combined with new byte. Check bits are output from CSR. Data and check bits are written to memory.

Table 2-10 Byte Write, Double Error Detected During Read

Normal operating mode	CSR 15 H is not set. No addresses or syndrome bits are logged. Old data is rewritten to memory, preserving double error at that location. New byte that was to be written is lost.
Diagnostic mode /protected	CSR 15 H is not set. No addresses or syndrome bits are logged. Old data is rewritten to memory, preserving double error at that location. New byte that was to be written is lost.
Diagnostic mode /unprotected	CSR 15 H is not set. No addresses or syndrome bits are logged. Error is ignored. New byte is combined with old byte and check bits are output from CSR.
Disable correction mode /protected	CSR 15 H is not set. No addresses or syndrome bits are logged. Old data is rewritten to memory, preserving double error at that location. New byte that was to be written is lost.
Disable correction mode /unprotected	CSR 15 H is not set. No addresses or syndrome bits are logged. Old data is rewritten to memory, preserving double error at that location. New byte that was to be written is lost.
Diagnostic and disable correction mode /protected	CSR 15 H is not set. No addresses or syndrome bits are logged. Old data is rewritten to memory, preserving double error at that location. New byte that was to be written is lost.
Diagnostic and disable correction mode /unprotected	CSR 15 H is not set. No addresses or syndrome bits are logged. Error is ignored. New byte is combined with old byte and check bits are output from CSR.

CHAPTER 3
TECHNICAL DESCRIPTION

3.Ø INTRODUCTION

This chapter provides a detailed technical description of the MS11-P MOS memory. Discussion begins with a description of the block diagram. The next part of the chapter is detailed operational descriptions of the memory system's major functional blocks. The final part of the chapter is descriptions of the memory system operations, aided by flow diagrams.

All circuit references, component labels, and signal names are from the MS11-P Field Maintenance Print Set, MP-Ø1477.

3.1 BLOCK DIAGRAM DESCRIPTION

This section introduces the functional blocks of the MS11-P memory system in a diagram that shows connections between the blocks (Figure 3-1). This section describes the memory system as the following four functional groups.

- UNIBUS
- Data bus
- Memory address selection
- Memory control circuits

NOTE

The section titles include the appropriate schematic page number in parentheses.

3.1.1 UNIBUS

The UNIBUS is the extended UNIBUS used in the PDP-11/24 and PDP-11/44 computers. It is an asynchronous, bidirectional parallel communications path between the central processor unit (CPU), memory, and peripheral controllers. The extended UNIBUS has 22-bit addressing for a 4 megabyte space address. It has the same control protocol, 16-bit wide data path, and separate data and address lines as other UNIBUSES.

By definition, the bus receivers and transceivers that connect the MS11-P memory system to the UNIBUS, are a part of the UNIBUS. However, this section has separate descriptions for the interface components.

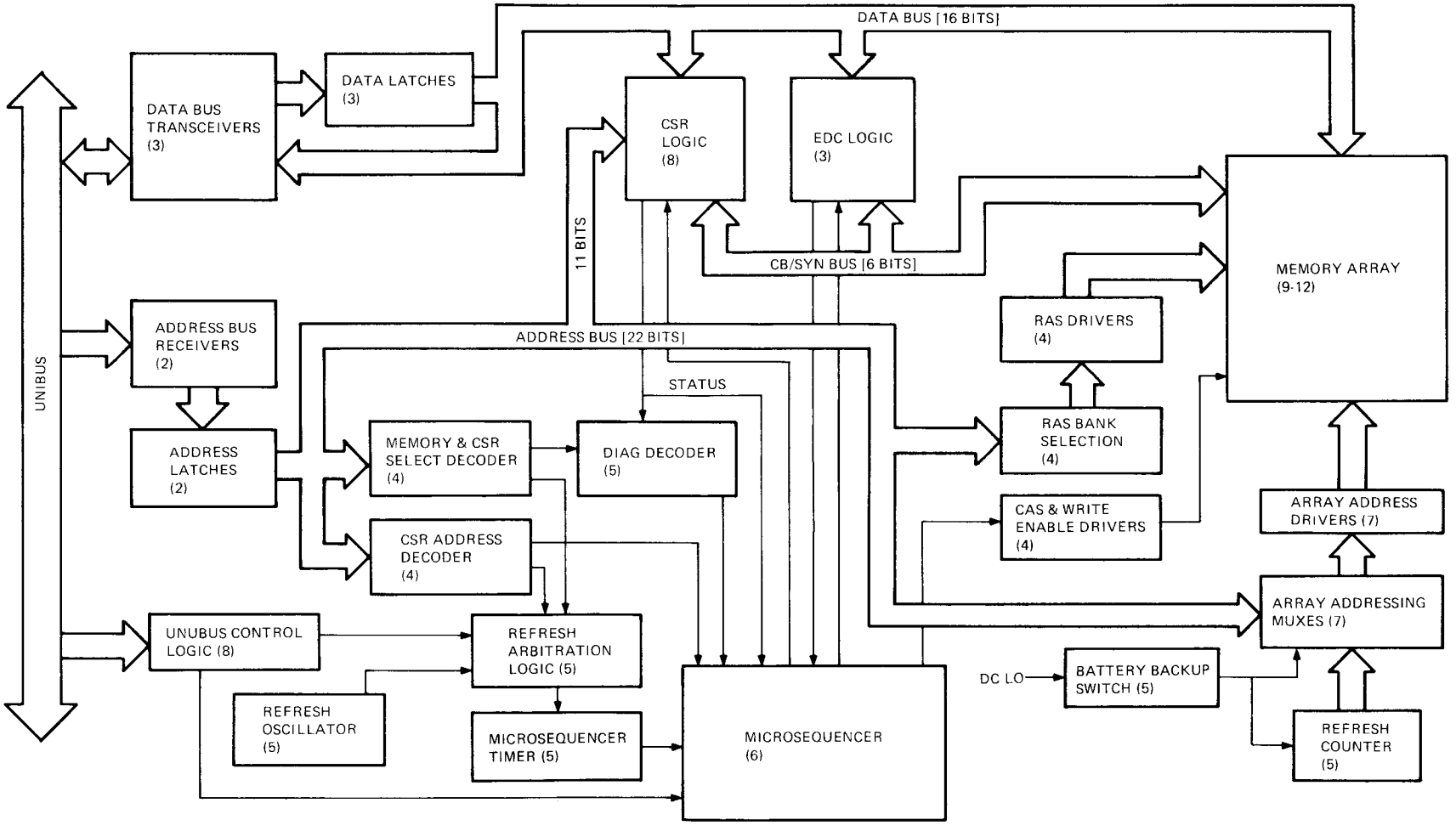


Figure 3-1 MS11-P Block Diagram

3.1.2 Data Bus

This section describes the wiring and components of the data bus. The data bus connects the UNIBUS data lines with the memory array and CSR.

3.1.2.1 Data Bus Transceivers (3) -- The data bus transceivers are integrated circuits designed to match the TTL signals in a system, to the controlled impedance and risetime characteristics of the UNIBUS. They can receive all the time, and they transmit when control signals from the UNIBUS indicate that the bus master wants data from memory.

3.1.2.2 Data Latches (3) -- The data latches hold data from the data bus transceivers. They supply that data to the rest of the data bus when needed. Therefore, logic on the data bus does not have to be rigidly timed to the UNIBUS cycle.

3.1.2.3 EDC Logic (3) -- The error detection and correction (EDC) logic is in a single IC. EDC logic connects to the memory system through the data bus and check bit/syndrome bit (CB/SYN) bus. A data word to be written enters EDC logic, which generates six check bits from the data. The check bits are written to the memory array along with the 16 data bits.

A data word and check bits that were read from memory enter the EDC logic. The EDC logic regenerates check bits from the read data, and compares the generated check bits with the read check bits. Any difference bits, called syndrome bits, indicate an error. If the error involves one bit only, the syndrome bits indicate the error location. The EDC logic corrects the error and passes corrected data to the data bus.

The EDC logic receives memory cycle commands from the microsequencer (Paragraph 3.1.4.4), and in turn sends error information to the microsequencer.

3.1.2.4 CSR Logic (8) -- The control and status register (CSR) logic is in a single IC. The CSR is 16-bits wide and is addressed as a location in the 128K extended UNIBUS I/O page. Paragraph 3.1.3.4 describes the addressing. The CSR connects to the memory system through the data bus and check bit/syndrome bit (CB/SYN) bus.

Some bits in the CSR are read/write. They provide control over memory system operation. Some bits control the microsequencer, and some control the CSR itself. Some bits provide status indications, and one also controls the uncorrectable error indicator LED on the edge of the memory module. Seven bits in the middle of the word can display three groups of data, depending on memory cycle and error conditions.

During a memory cycle that involves an error, the CSR stores the following information about the cycle.

- The address of the 1K block in which the error occurred
- The check bits or syndrome bits

For diagnosis, the CSR allows insertion of externally provided check bits onto the CB/SYN bus for writing to memory.

The CSR provides status information to the microsequencer (Paragraph 3.1.4.4), and in turn receives memory cycle information from the microsequencer. Figure 2-4 in Chapter 2 shows CSR bit assignments in detail.

3.1.3 **Memory Address Selection** -- This section describes parts of the memory system that select a single data location to be read or written.

3.1.3.1 **Address Bus Receivers (2)** -- The address bus receivers are integrated circuits designed to match the TTL signals in a system, to the controlled impedance and risetime characteristics of the UNIBUS. They are actually transceivers, but are used for receiving only.

3.1.3.2 **Address Latches (2)** -- The address latches hold addresses from the address bus receivers. One latch supplies address bits A21:A17 to the RAS bank selection circuit, which needs a stable signal during an entire memory cycle. The other latch supplies column address bits A16:AØ9 to the array addressing multiplexers, because the RAMs latch the row addresses first, then the column addresses after a delay. The UNIBUS may not keep the address bus stable long enough for both sets of addresses to be latched in the RAM.

3.1.3.3 **Memory and CSR Select Decoder (4)** -- The memory and CSR select decoder has two ROMs that compare the high eight address bits with the eight switch settings that control the memory system's starting address. The ROMs supply signals that indicate whether or not the following conditions exist.

- Is the memory system being addressed?
- Is the lower 32K of the memory system being addressed?
- Is the upper or lower 16K of the lower 32K of the memory system being addressed?
- Is the CSR address (high bits of the extended UNIBUS I/O page address space) being addressed?

3.1.3.4 CSR Address Decoder (4) -- The CSR address decoder supplies signals that indicate that the CSR is being addressed. The extended UNIBUS has 16 standard addresses available for CSRs of MS11-family memory systems. The high bits of these addresses are preset in the MS11-P's decoders. Only the low four bits are compared to select a CSR according to the switch settings.

3.1.3.5 RAS Bank Selection (4) -- The RAS bank selector is a ROM that decodes five address inputs to eight outputs. The RAS banks are the first level of address decoding in the memory system. The rest of the decoding occurs inside the RAMs with 16 bits of row and column addressing. There are five inputs to the bank selector because the memory starting address can be placed on a boundary where more than one bit must change to select a new bank.

An initialization/refresh signal is also an input to the bank selector because, during initialization or refresh, all eight banks need to be selected at the same time.

3.1.3.6 RAS Drivers (4) -- The RAS drivers supply RAS signals to the memory array, with only one bank receiving the signal at a time (except during refresh). The drivers are high power output integrated circuits, with small value resistors in series with their outputs, to minimize reflections in the memory array wiring.

3.1.3.7 CAS and Write Enable Drivers (4) -- These drivers are the same as the RAS drivers. All RAMs in the array get the CAS signal at the same time. When write enable (WE) is used, all the RAMs in the array receive WE at the same time.

3.1.3.8 Array Addressing Muxes (7) -- The array addressing multiplexers supply the memory array with one of four groups of eight address bits: read/write row addresses, read/write column addresses, initialization/refresh row addresses, and initialization column addresses.

3.1.3.9 Array Address Drivers (7) -- These drivers are the same as the RAS drivers. They supply signals from the array addressing multiplexers to the memory array.

3.1.3.10 Memory Array (9--12) -- The memory array is 176 65536 X 1 bit MOS dynamic RAM integrated circuits. Each RAM has 8 address lines which accept a 16-bit address in two parts (row and column). All address, data, CAS, and write enable lines are connected together in the complete array. Only the RAS lines are separated into 8 banks of 22 RAMs each. Each bank has 16 RAMs for data and 6 RAMs for check bits. The data input and output lines on each RAM are connected, and a system called early write prevents conflicts between the lines.

3.1.4 Memory Control Circuits

The memory control circuits select the time and type of memory operation, and control the memory system's many parts to make it perform its function.

3.1.4.1 UNIBUS Control Logic (8) -- The UNIBUS is the source of all requests for service by memory, either reading or writing. The UNIBUS control logic supplies information about the state of the UNIBUS, to the memory system. That information lets memory accept or supply data to the UNIBUS when the UNIBUS is ready.

3.1.4.2 Microsequencer Timer (5) -- The microsequencer timer is a delay line oscillator that provides the microsequencer with one primary and one secondary clock signal. The primary clock runs with a 110 ns period, and the secondary clock has the same period, but starts 60 ns later. The timer runs only when a memory cycle is being performed. The timer starts when either a refresh cycle, CSR access cycle, or memory access cycle is requested. The refresh arbitration logic controls when the timer starts.

3.1.4.3 DIAG (Diagnostic) Decoder (5) -- The diagnostic decoder uses signals from the CSR, the memory, and CSR select decoder to select the type of memory cycle to perform. For example, if the addressed location is not in the memory's protected region, and the memory is in a mode with correction disabled, the microsequencer is sent to a routine that does not correct errors.

3.1.4.4 Microsequencer (6) -- The microsequencer is the memory system's controller. Its output signals control the timing of nearly every function in the system. The microsequencer is a ROM that contains routines, or programs, for each of the many different types of memory cycles that can occur. The steps of the routine change when the microsequencer timer supplies a clock pulse. Several inputs from the CSR, refresh arbitration logic, memory select logic, diagnostic decoder, and UNIBUS address and control signals select the routine. These inputs are combined into a starting address for the ROM. There is a different routine for each combination of input signals. This gives the memory system its wide range of operating modes.

3.1.4.5 Battery Backup Switch (5) -- The battery backup switch monitors the UNIBUS DC LO signal. If that signal falls, the switch prevents memory cycles from starting, and only allows refresh cycles to continue.

The switch logic includes a multiplexer that provides the signals that control row, column, RAS, and CAS timing for the memory array. In normal operation, the timing for these signals comes from the microsequencer. During battery backup, the multiplexer selects timing for RAS from the refresh oscillator, while it holds the other signals unchanged.

3.1.4.6 Refresh Oscillator (5) -- The refresh oscillator is a simple analog timer circuit. It provides a signal to request a refresh cycle every 13.3 microseconds. At that rate, all 128 rows in all memory ICs are refreshed within the required two milliseconds. A flip-flop latches the request into the refresh arbitration logic.

3.1.4.7 Refresh Arbitration Logic (5) -- The refresh arbitration logic monitors the states of the memory system, UNIBUS, and refresh request logic. This logic prevents a refresh cycle from starting until a memory cycle finishes. It also prevents a memory cycle from starting until a refresh cycle finishes.

3.1.4.8 Refresh Counter (5) -- The refresh counter is two eight-bit counters. During refresh, one counter supplies one of 128 counts for the memory array's row address.

This counter also supplies addressing for memory system initialization. A memory data location with all zeros in it has a check bit pattern of ØØ1ØØ. This pattern must be loaded into the check bit part of each location in the memory array.

During initialization, both counters operate together to provide row and column addressing to all 64K locations in each RAM IC. The EDC logic provides the 22 bits of data. All the RAS and CAS lines cycle at the same time, writing data into every RAM on the module at the selected RAM location.

Initialization timing comes from the refresh oscillator and microsequencer timer. During initialization, no other memory cycles are allowed, so each new refresh oscillator pulse requests another initialization to a location. Therefore, the initialization process takes 64K X 13.3 microseconds, or approximately 9ØØ milliseconds.

3.2 DETAILED DESCRIPTIONS

This section describes in detail the complex functional blocks in the memory system. The following blocks are described.

Memory ICs and memory array
Error detection and correction (EDC) logic
Control and status register (CSR) logic
Memory and CSR select decoder
UNIBUS control logic
Microsequencer timer
Diagnostic decoder
Microsequencer
Battery backup switch
Refresh arbitration logic

3.2.1 Memory ICs and memory array

The MS11-P memory system uses 64K dynamic RAMs to provide a one megabyte storage capacity. This section explains the influence of memory devices on the memory system design. Memory manufacturers' documentation provides more detail. This information is provided as an overview.

3.2.1.1 Dynamic Memory with Multiplexed Addressing -- The 4164 64K dynamic random access memories (DRAM) used in the MS11-P have several features to note.

They are dynamic devices. Therefore, they need regular refreshing to hold their data. The memory system has circuitry that provides this refreshing on a shared basis with data accesses.

The DRAMs have multiplexed address inputs. The 64K DRAM needs 16 address bits to supply a unique address for each memory location. To keep the package and pin needs small, the address bits are divided into two groups called row and column addresses. The memory IC's inner structure is arranged in rows and columns so the address division is convenient. Refer to Figure 3-2.

They have data inputs and outputs that are tied together in the MS11-P. Supplying write enable (WE) before column address strobe (CAS) allows data to be written to the DRAM while the data output stays tri-stated. CAS alone causes data to appear at the data output, while the write drivers are disabled. Having the DRAMs share input and output lines simplifies circuit board layout.

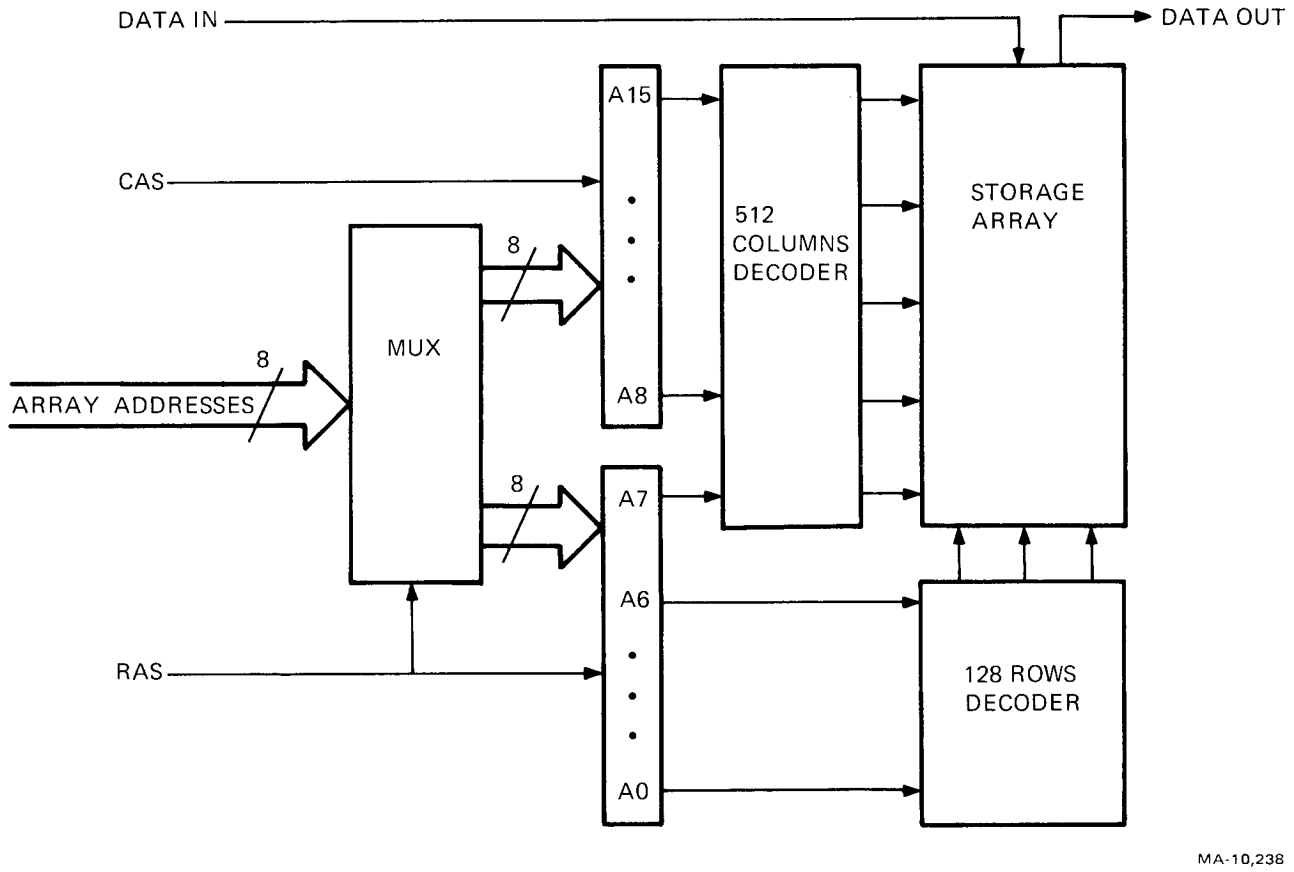


Figure 3-2 DRAM Addressing Concept Block Diagram

The 4164 DRAM reserves pin 1 for compatibility with future 256K DRAM designs. When this IC was designed the previous type was the 4116. That IC used three power supplies. The 4164 has charge pumps to supply the added voltages, which saves two pins over the 4116. One pin is needed for address bit 8 in the 4164. The other pin is for address bit 9 in a 256K DRAM. The internal power supplies, however, must be started up with added RAS signals before the DRAMs can be used at power up.

Refresh circuitry for the 64K DRAM is functionally compatible with the 16K DRAM circuitry. Each location's need for refresh within two milliseconds stays the same. This is an important feature because the reduction in storage cell size and charge capacity would suggest the need for an increased refresh rate. And, the number of refresh cycles remains the same at 128 within two milliseconds. This is important because the larger storage array would suggest a doubling of the number of rows that need to be refreshed. However, the internal layout of the 4164 is not square, and the 16 bits of address are not evenly divided between rows and columns. The first seven bits of address are row addresses and take care of refresh. But, the eighth bit that is strobed with RAS is actually stored for use in column decoding. Then, the second group of eight bits is strobed with CAS for a total of nine bits to select one of 512 columns.

3.2.1.2 Check Bits and Error Correction -- The memory system stores 22 bits for each 16-bit data word. The additional six bits are check bits that allow memory to detect and correct most errors. Soft errors caused by subatomic particles are thought to be more likely in memories based on the 64K DRAM, than in previous memories. This difference makes the addition of an error correcting system more important. But, the additional cost of check bit storage and EDC circuitry has also made the complete memory system more reliable than older systems with the same capacity and greater cost.

3.2.2 Error Detection and Correction (EDC) Logic

One IC, called the AM2960 contains all the error detection and correction circuitry. This section describes the EDC architecture.

Figure 3-3 shows the EDC block diagram, which includes the following components.

- Data input latch
- Check bit input latch
- Check bit generation logic
- Syndrome generation logic
- Error detection logic
- Error correction logic
- Data output latch
- Control logic

The rest of this section describes the EDC functional blocks. Uppercase words are EDC inputs and outputs.

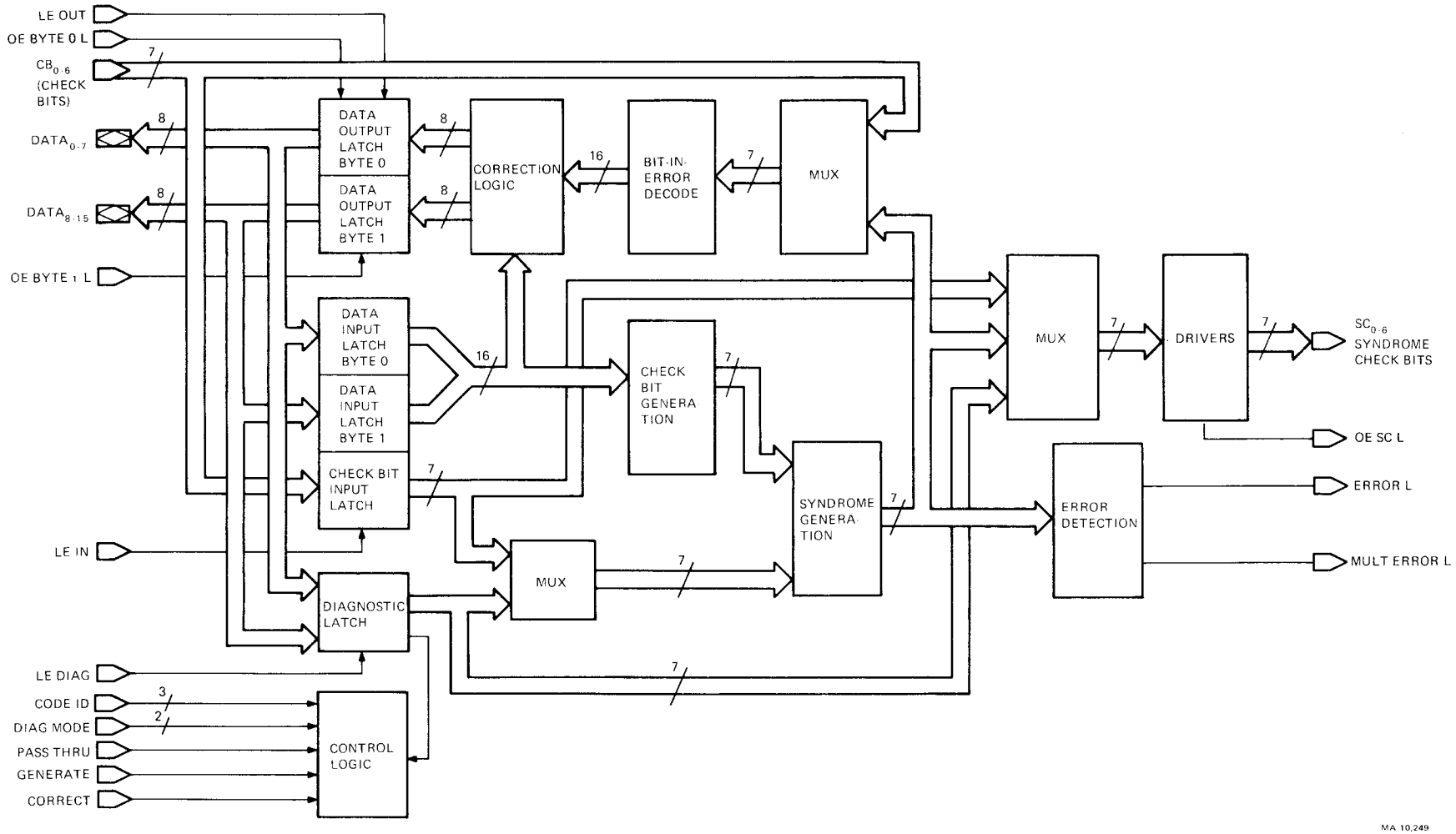


Figure 3-3 EDC Logic Block Diagram

Data Input Latch -- 16 bits of data are loaded from the bidirectional DATA lines under control of the latch enable input, LE IN. Depending on the control mode, the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch -- Seven check bits are loaded under LE IN control. (The MS11-P only uses six check bits.) Check bits are used in error detection mode and error correction mode.

Check Bit Generation Logic -- This circuit generates check bits for the 16 bits of data in the data input latch. The check bits are generated according to a modified Hamming code (Table 3-1). (Hamming codes are named for the mathematician who developed them.)

Syndrome Bit Generation Logic -- In both error detection and error correction modes, this circuit compares check bits read from memory with a set of new check bits generated from data read from memory. If the sets of check bits are the same, then there are no errors. If any bits are different, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive OR of the two sets of check bits. If the two sets of check bits are identical (there are no errors) the syndrome bits are all zeros. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit in error.

Table 3-1 16-Bit Modified Hamming Code Check Bit Encode Chart

Generated Check Bits	Parity	Participating Data Bits Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
CØ	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (NXOR)	X			X	X			X		X	X			X		X
C2	Odd (NXOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

NOTE: Check bits are generated as either an XOR or NXOR for the eight data bits noted by X in the table.

Error Detection Logic -- This circuit decodes the syndrome bits generated by the syndrome generation logic. If there are no errors in either input data or check bits, ERROR L and MULT ERROR L outputs remain high. If one or more errors are detected, ERROR L goes low. If two or more errors are detected, both ERROR L and MULT ERROR L go low (Table 3-2).

Error Correction Logic -- For single errors, the error correction logic complements (corrects) the single data bit in error. This corrected data is loadable into the data output latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to generate mode.

Table 3-2 Syndrome Decode to Bit-In-Error

Syndrome Bits SX	SØ	S1	S8	Ø	1	Ø	1	Ø	1	Ø	1
			S4	Ø	Ø	1	1	Ø	Ø	1	1
			S2	Ø	Ø	Ø	Ø	1	1	1	1
Ø	Ø	Ø		*	C8	C4	T	C2	T	T	M
Ø	Ø	1		C1	T	T	15	T	13	7	T
Ø	1	Ø		CØ	T	T	M	T	12	6	T
Ø	1	1		T	1Ø	4	T	Ø	T	T	M
1	Ø	Ø		CX	T	T	14	T	11	5	T
1	Ø	1		T	9	3	T	M	T	T	M
1	1	Ø		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

Key
* Means no errors detected

A number means the location of the single bit-in-error
T Means two errors detected
M Means three or more errors detected

Notes:
Syndrome bits (SØ, etc.) are formed by a comparing the check bits read from memory and the new check bits generated on the data read from memory.

A single error or a multiple error causes an odd number of syndrome bits to go high. A double error causes an even number to go high.

Data Output Latch -- The data output latch stores the result of an error correction operation. The latch is loaded from the correction logic under control of the data output latch enable signal, LE OUT. The data output latch may also be loaded directly from the data input latch under control of the PASS THRU contol input.

The data output latch is split into two eight-bit (byte) latches, which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch -- This 16-bit latch is loadable from the bidirectional data lines under control of the diagnostic latch enable signal, LE DIAG. The diagnostic latch holds check bit information in one byte, and control information in the other byte. The diagnostic latch supplies control commands to the EDC when the EDC is in internal control mode. The latch supplies check bits when the EDC is in one of the diagnostic modes.

Control Logic -- The control logic selects the EDC operating mode. Typically, the control logic gets its commands from the external control inputs. However, in internal control mode, the control signals are read from the diagnostic latch.

3.2.3 Control and Status Register (CSR) Logic

The control and status register (CSR) controls MS11-P memory system operation. It stores error information and controls memory's diagnostic modes. It connects to the memory system with tri-state data bus transceivers and check bit/syndrome bus transceivers. Address information is input from the memory address bus, and latched into an internal register. There are three control signal inputs, a chip enable, and an initialization signal. There are also six status output bits that define the memory's operating mode.

Refer to the CSR block diagram, Figure 3-4. The CSR has two bidirectional ports. The memory data bus port connects the CSR to the memory array. Most of the CSR's internal registers are written and read through this port. The check bit/syndrome bus port connects the CSR to the error detection/correction logic and check bit storage array. Check bit or error syndrome information can be written or read through this port.

The CSR has an input only port, which connects part of the address bus to an internal register, which stores some information about the address of a location where an error occurred. There is an output only port which provides status information, loaded by the CPU, to the memory system.

The CSR has five control inputs. Table 3-3 shows the three cycle-select signals that are internally decoded to select one of eight cycle types.

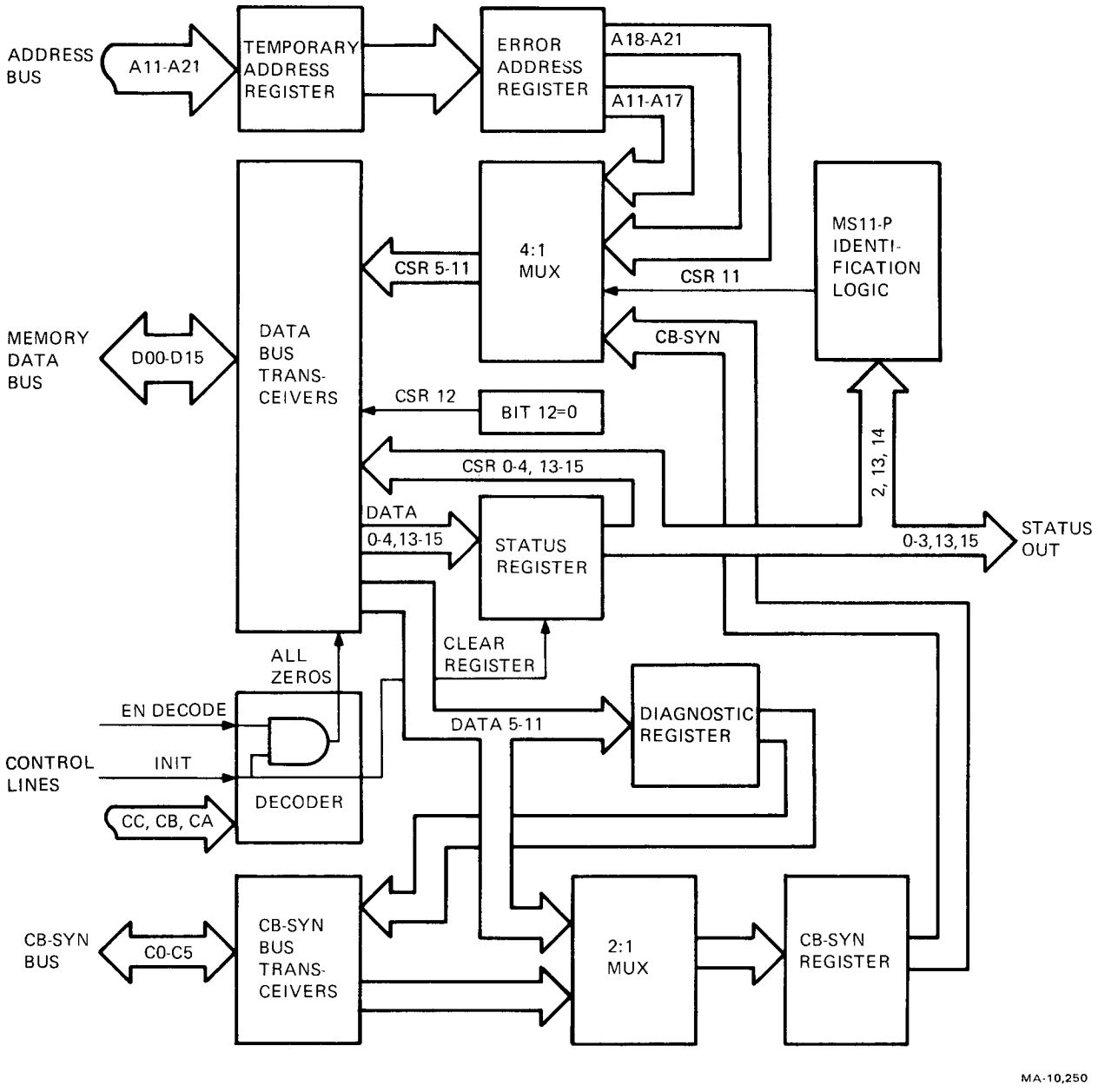


Figure 3-4 CSR Block Diagram

Table 3-3 CSR Cycle Selection

Cycle	CC H	CB H	CA H
Cb-Syn In	Ø	Ø	Ø
Double error log	Ø	Ø	1
Single error log	Ø	1	Ø
Diagnostic out	Ø	1	1
Write CSR-diagnostic	1	Ø	Ø
Write CSR	1	Ø	1
Read CSR	1	1	Ø
Clock temporary address	1	1	1

Enable Decode (EN DECODE H), asserted with the cycle select signals, starts a cycle in the CSR. Init, asserted alone, clears the status out bits. Init, asserted with Enable Decode, drives the data bus to all zeros.

The rest of this section describes the CSR functional blocks.

Decoder -- The three cycle select signals are input to the decoder to select one of eight cycle types. The assertion of EN DECODE H then enables the decoder.

Temporary Address Register -- Address information is input from the memory address bus into this 11-bit register on a clock temporary address cycle. Latching occurs on the falling edge of EN DECODE H.

Error Register -- The contents of the temporary address register are transferred to the error register on a single or double error log cycle (Table 3-4).

4:1 Mux -- This multiplexer selects one of four internal data sources to be placed on CSR 5 H -- CSR 11 H during a read CSR cycle. The multiplexer selects the sources according to Table 3-5.

Data Bus Transceivers -- The data bus transceivers are tri-state I/O devices that interface the CSR to the memory data bus.

Status Register -- The status register is an internal eight-bit register. It is loaded by a write CSR or write CSR diagnostic cycle and read by a read CSR cycle. CSR Ø--4 and CSR 13--15 are input from the data bus transceivers to the status register, and CSR Ø, 1, 2, 3, 13, and 15 are available at the status out port. CSR 4 H is also set by a single error log cycle, and CSR 15 H is set by a double error log cycle.

Table 3-4 Error Register Operation

CSR 2 H	CSR 15 H	Single Error Log	Double Error Log
Ø	Ø	Transfer	Transfer
Ø	1	No transfer	Transfer
1	Ø	No transfer	No transfer
1	1	No transfer	No transfer

Table 3-5 Multiplexer Control

CSR 2 H	CSR 14 H	CSR 5 -- CSR 11 H
Ø	Ø	A11 -- A17
Ø	1	A18 -- A21
1	Ø	Cb-Syn
1	1	Cb-Syn*

*CSR 11 H is read as one if CSR 2, 13, and 14 are set to one.

2:1 Mux -- The 2:1 multiplexer controls input to the Cb-Syn register. A Cb-Syn In cycle (CC H equals Ø) selects data from the Cb-Syn bus transceivers, while a write CSR diagnostic selects CSR 5--1Ø from the data bus transceivers.

Cb-Syn Bus Transceivers -- The check bit/syndrome (Cb-Syn) bus transceivers are tri-state I/O devices that connect the CSR to the Cb-Syn data bus.

Diagnostic Register -- This internal six-bit register holds the contents of CSR 5--1Ø. It is loaded on a write CSR or write CSR diagnostic cycle. It can be read on the Cb-Syn bus by a diagnostic out cycle.

Cb-Syn Register -- The Cb-Syn register is an internal six-bit register. It can be written from the Cb-Syn bus by a Cb-Syn In cycle, or from the data bus by a write CSR diagnostic cycle. It is also loaded from the Cb-Syn bus by a single- or double-error log cycle whenever CSR 2 H equals Ø. The Cb-Syn register contents are read as CSR 5--1Ø H during a CSR read cycle, when CSR 2 H equals 1.

3.2.4 Memory and CSR Select Decoder

This circuit indicates three different conditions to the memory system. It indicates that an address in the memory system is being accessed by the bus; that the accessed location is in the lower or upper 16K words of the first 32K words in the module; or that the accessed location is in the range of CSR addresses in the I/O page of the extended UNIBUS.

3.2.4.1 Memory Address Selection -- Each of the 512K words on the memory module can be individually addressed from the UNIBUS. In a simple system with memory starting at location Ø, the low 2Ø address bits on the bus select one of the words for reading or writing. However, there are three complications to this apparently straightforward addressing method.

The first complication is that the extended UNIBUS is able to address four times the amount of memory on an MS11-P module. The bus needs 22 bits to specify each unique address. Each memory module in the system decodes all 22 bits to determine if the addressed location is in its array.

The second complication is that the MS11-P must share the extended UNIBUS with other, smaller memory systems. One of those other systems can have its first, or starting, address set to any 4K boundary in the address space. This means to keep memory locations on the bus contiguous (each bus address represents a data location, with no unused addresses between locations) the starting address of each memory module must be settable to nearly any value. The MS11-P compromises with a minimum 8K boundary. Any system that has both kinds of memories must use 8K boundaries.

Because the starting address for the 512K memory can be almost anywhere in the address space, all 22 bits of the address bus are needed for every location. The high bits do not select modules in just the simple way described above. A module's address space can extend across 512K boundaries, so the high bits can change between locations in the same module.

The third complication is that the extended UNIBUS does not allow memory locations to be in the top 128K words of the address space. That space has other uses. Each memory module has a CSR located in that address space. The module's own address decoding must make sure that no memory accesses occur in that address space, but must allow an I/O access to its own CSR. Information about the type of access is provided by signals on the UNIBUS. Each module on the bus needs a unique I/O address that accesses its CSR. Each module has switches to select the address from a limited range of standardized bus locations.

The MS11-P memory and CSR select decoding circuitry recognizes an address in the CSR range, and the CSR address decoder compares four bus address bits with the switch settings, to access the specific module's CSR.

3.2.4.2 Memory Address Decoder -- The memory address decoder uses ROMs to decide whether a bus address is accessing a location within the module's memory array, or in another location with the same low bits on another memory module in the extended UNIBUS address space. The memory address decoder also tells the memory system when the addressed location is in the first or second 16K words of memory, for diagnostic purposes. Finally, it decodes the highest bits of the CSR address by indicating when the upper 128K segment of the extended UNIBUS is being addressed.

The ROM decoder has two sections (the two ROMs). Each section detects different information about the bus address. The 128K ROM (E33) determines which 128K word segment of the UNIBUS address is being addressed by the bits on the bus. The 8K ROM (E39) determines which 8K word segment of the bus is being addressed.

Figure 3-5 shows how the extended UNIBUS address space can be divided into 16 segments of 128K words each. Table 3-6 shows how the 128K ROM examines the high four bits on the bus to determine which 128K segment is being addressed. There are four switch inputs to the ROM. The ROM is programmed so its output has the effect of comparing the bus address with the switch inputs. If the high four bits in the bus address are within four, four-bit counts of the value on the switch inputs, the 128K ROM MEM LO data output goes high. If the starting address (SA) of the memory system is on a 128K word boundary in the extended UNIBUS address space, that is all the memory decoding needed. The 4 counts (out of 16) correctly indicate where in the address space the 512K word memory array is located.

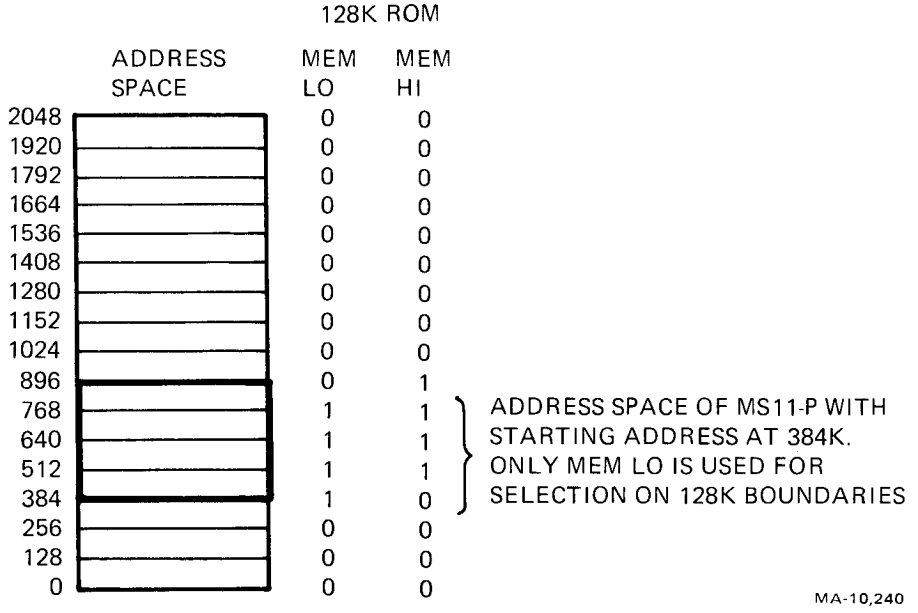


Figure 3-5 Address Space on 128K Boundary

However, the decoding process is more complicated when the memory array begins at some address that is on an 8K word boundary, away from the 128K boundaries.

Figure 3-6 shows the 512K address range of the memory array starting halfway between 128K boundaries, at the 64K point. Above the 128K boundary, but below the 64K starting address (A17 -- A14 = 0000 > 0111), the 128K ROM puts a high signal on its LO data output, because the address is in the first 128K range. However, the 8K ROM puts a low signal on its LO data output, because the low four bits of the address are accessing memory below the array's starting address. The AND combination of the two different LO outputs is a low signal that means the memory is not being accessed. At, or above, the 64K starting address (A17 -- A14 = 1000 > 1111), the 8K ROM puts a high signal on its LO output. The AND combination of the two high LO outputs is a high signal that means the memory is being accessed.

In the next three 128K segments, both 128K ROM MEM LO and MEM HI outputs are high. When the 8K ROM has inputs in the 8K boundary address space below the starting address, its MEM HI output is high. With the MEM LO output high for addresses above the starting address, any address in the three 128K segments has either a high or low output that can AND with one of the two outputs from the 128K ROM.

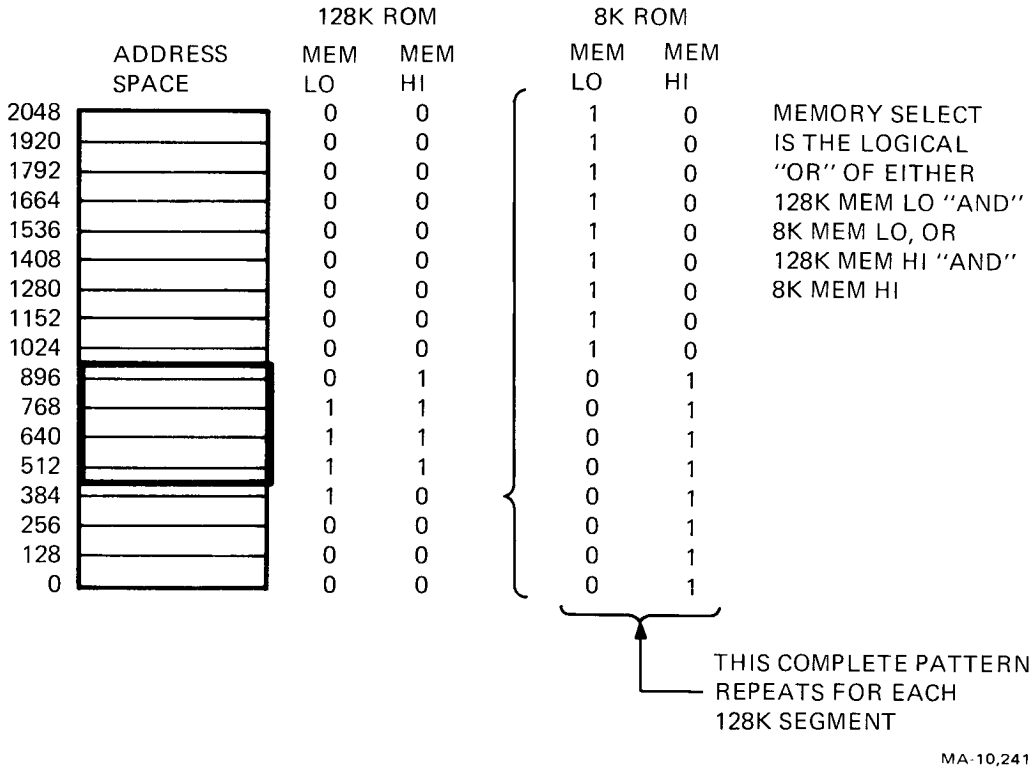


Figure 3-6 Address Space on 8K Boundary

Table 3-6 shows the outputs of the 128K ROM and 8K ROM together. The table shows how the different combinations of outputs are ANDed together. If either ANDed output goes high, the address on the bus is a valid address for a location in the memory module. The microsequencer is allowed to process a memory service request, and the memory array uses the lower bus address bits A19 -- A01 directly, to access a location.

Table 3-6 Address Decoder ROM Outputs

128K ROM				8K ROM					
Address Switches 21201918	**Address Bus 21201918**	**Mem LO**	**Mem HI**	**Address Switches 17161514**	**Address BUS 17161514**	**Mem LO**	**Mem HI**	**Both ROM Outputs ANDed LO**	**HI**
High bits cycle through 128K segments, low bits fixed at starting address.									
0 0 1 0	0 0 0 0	0	0	0 0 0 0	0 0 0 0	1	0	0	0
0 0 1 0	0 0 0 1	0	0	0 0 0 0	0 0 0 0	1	0	0	0
0 0 1 0	0 0 1 0	1	0	0 0 0 0	0 0 0 0	1	0	>1	0
0 0 1 0	0 0 1 1	1	1	0 0 0 0	0 0 0 0	1	0	>1	0
0 0 1 0	0 1 0 0	1	1	0 0 0 0	0 0 0 0	1	0	>1	0
0 0 1 0	0 1 0 1	1	1	0 0 0 0	0 0 0 0	1	0	>1	0
0 0 1 0	0 1 1 1	0	1	0 0 0 0	0 0 0 0	1	0	0	0
0 0 1 0	1 0 0 0	0	0	0 0 0 0	0 0 0 0	1	0	0	0
High bits fixed at starting address, low bits change from below starting address at 64K to above starting address, then high bits change to upper limit of module address range:									
0 0 1 0	0 0 1 0	1	0	1 0 0 0	0 1 1 1	0	1	0	0
0 0 1 0	0 0 1 0	1	0	1 0 0 0	1 0 0 0	1	0	>1	0
0 0 1 0	0 0 1 0	1	0	1 0 0 0	1 0 0 1	1	0	>1	0
0 0 1 0	0 0 1 0	1	0	1 0 0 0	1 1 1 1	1	0	>1	0
0 0 1 0	0 0 1 1	1	1	1 0 0 0	0 0 0 0	0	1	>0	1
0 0 1 0	0 1 1 0	0	1	1 0 0 0	0 0 0 0	0	1	>0	1
0 0 1 0	0 1 1 1	0	0	1 0 0 0	0 0 0 0	0	1	0	0

Note: Arrows point to ANDed outputs that enable module.

3.2.4.3 Other Outputs from the Decoder -- Signals NA 15 (normalized address bit 15) H and L are the ROM E39 outputs that indicate an address change from one 16K words region of memory to the next (refer to Paragraph 3.2.7 for an explanation). Normalized means the 16K word boundary is counted from the first location in the memory array, not the UNIBUS address boundary. There are two bits of information available in these two signals. They indicate three things: one or the other signal asserted means the address is in either the first two 8K word segments, or the second two 8K word segments. Neither signal asserted means the address is above 32K words. (Both signals cannot be asserted.)

However, the signals only come from the 8K ROM, so they can only indicate segments in a 128K word range. Therefore, the signals repeat four times in the address range of the complete memory. Two other signals called 1ST 32K HI and 1ST 32K LO, that come from both ROMs, clarify which repetition indicates the real start of memory. They AND together and provide outputs when the 128K ROM indicates that an address is in the first 128K words of memory. With two signals, the memory can handle starting addresses that are within 32K of the top of a 128K segment. This is like the method described in Paragraph 3.2.3.2 for memory module selection.

The signal CSR HI BITS indicates that all address bits A21 -- A14 are high on the bus. Bits A21 -- A18 high mean that the bus is addressing the top 128K words, which is the I/O page. Only the CSR can be accessed in this address space. The signal goes to the CSR address decoder.

3.2.5 UNIBUS Control Logic

The UNIBUS control signals, both incoming and outgoing, pass through this circuitry. This section describes each of the UNIBUS signals, and their origins or effects on the memory system. All UNIBUS signals are asserted low. Most of the signals appear on page MSØ8 of the print set. The MS11-P is never bus master and therefore passes all NPR and grant signals without change.

BUS DC LO (Input) -- Memory receives DC LO. DC LO indicates that the +5 volt dc power supply is about to fail. The memory completes any current operation and enters battery backup mode.

BOOT EN (Input) -- Boot enable, when held low, allows DC LO to start ECC initialization.

BUS INIT (Input) -- Bus initialization is a signal from the UNIBUS that clears the CSR status register, and, if received while MSØ6 EN DEC H is high, sets the CSR data bus outputs to all zeros.

BUS MSYN (Input) -- Master sync is issued by the bus master and received by the memory system. Its assertion requests memory to perform the function defined by CØ and C1. Its negation indicates that the master considers the data transfer concluded.

BUS CØ, BUS C1 (Inputs) -- These signals tell the memory system what kind of bus cycle is to be performed (Table 3-7). They enter the system at E48 (page MSØ2). They control system operation by modifying the microsequencer starting address (page MSØ6).

BUS AC LO (Output) -- The memory system issues AC LO to tell the bus that the memory is not ready to function. AC LO is asserted during memory ECC initialization. The initialization control circuit is shown as part of the UNIBUS control logic. Refer to ECC initialization below.

BUS SSYN (Output) -- Slave sync is issued by the memory system. The logic that produces it is in E6 (page MSØ6 of the print set). Its assertion tells the bus master that memory has concluded its part of the data transfer. For a DATI or DATIP, the requested data is placed on the data lines; for a DATO or DATOB, the data on the data lines is accepted.

Slave sync's negation informs all bus devices that memory has concluded the data transfer. For data in functions, negation of SSYN indicates that negation of MSYN is received, and data removed from the data lines. For data out functions, negation of SSYN indicates that negation of MSYN is received.

BUS PB (Output) -- Parity error indicator PB is set on an uncorrected error, if allowed by CSR bit zero. PB is gated by SSYN and appears on the bus at the same time as the uncorrected data. The logic that produces it is in E6 (page MSØ6 of the print set).

ECC Initialization -- This circuit, while not part of the UNIBUS, is shown in the UNIBUS control logic because its operation is so involved with the UNIBUS. The control circuit is a pair of flip-flops that are clocked by address bits from the memory array when it is being initialized. Bit A16 toggling means that all 64K locations in each RAM have been accessed by the refresh/initialization counter (page MSØ5). The circuit actually waits until bit A9 toggles a second time before it ends the initialization process. These extra 256 accesses in the low part of the memory array make sure that those locations are

Table 3-7 UNIBUS Cycle Control

Function	C1	CØ
DATI	Ø	Ø
DATIP	Ø	1
DATO	1	Ø
DATOB	1	1

successfully initialized. The RAMs require some number of RAS pulses at power-up to bring up their internal charge pump voltage converters. But, the array gets its first RAS pulses at initialization. Therefore, the first several locations accessed, are probably not initialized.

ECC initialization is started by +5 VBB (the battery backup side of the power supply) coming up at E1-7. This is the normal process. If battery backup is not being used, both power supply connections are tied together, and E1-7 still starts initialization. However, initialization is possible when main power is turned on, even if battery backup is available. Holding BOOT EN low during power-up starts initialization by passing DC LO through E1-4 to E2-9.

The WAKE UP signals from the initialization start signal clear the refresh/initialization counter to start the count at zero and disable the RAS, CAS, and WE drivers. This prevents writing to the memories until the system is stable.

3.2.6 Microsequencer Timer

Refer to the simplified diagram (Figure 3-7) and the timing diagram that goes with it (Figure 3-8). The central part of the timing circuit is three gates: a delay line with two taps, and an inverter. The circuit's initial condition has the delay line outputs low. The inverter at T40 has a high output. E4-13 is high so E4-9 inverts and passes any signal. E5-11 is high and E5-10 is also high, although it is active low (in this simplified diagram). E5-9 is low. E5-8 is high. E4-1, -5, and -4 are high, and E4-6 is low.

A low-going pulse from the refresh arbitration logic makes E4-6 go high. NA SEL L from the microsequencer goes low at E5-10. E4-6 drives E4-9 high, which makes E4-8 go low. The low input to E4-5 keeps E4-6 high after the initiating pulse ends. After a 40 nanosecond delay, the original high input to the delay line arrives at T40. T40 goes high and makes E4-13 low. E4-8 goes high so E4-6 goes low.

After another 40 ns, the low input to the delay line arrives at T40. T40 goes low and makes E4-13 go high so E4-9 inverts and passes any signal. E5-11 is also high. After another 20 ns, the original high input to the delay line arrives at T100. T100 goes high at E5-9. E5-8 makes E4-4 go low, which makes E4-6 go high. Now a new cycle starts.

At the start of the last clock cycle of a memory cycle, NA SEL L from the microsequencer goes high. Then, when T100 goes high, E5-8 cannot go low, so E4-6 does not go high to start another cycle. The timer stops.

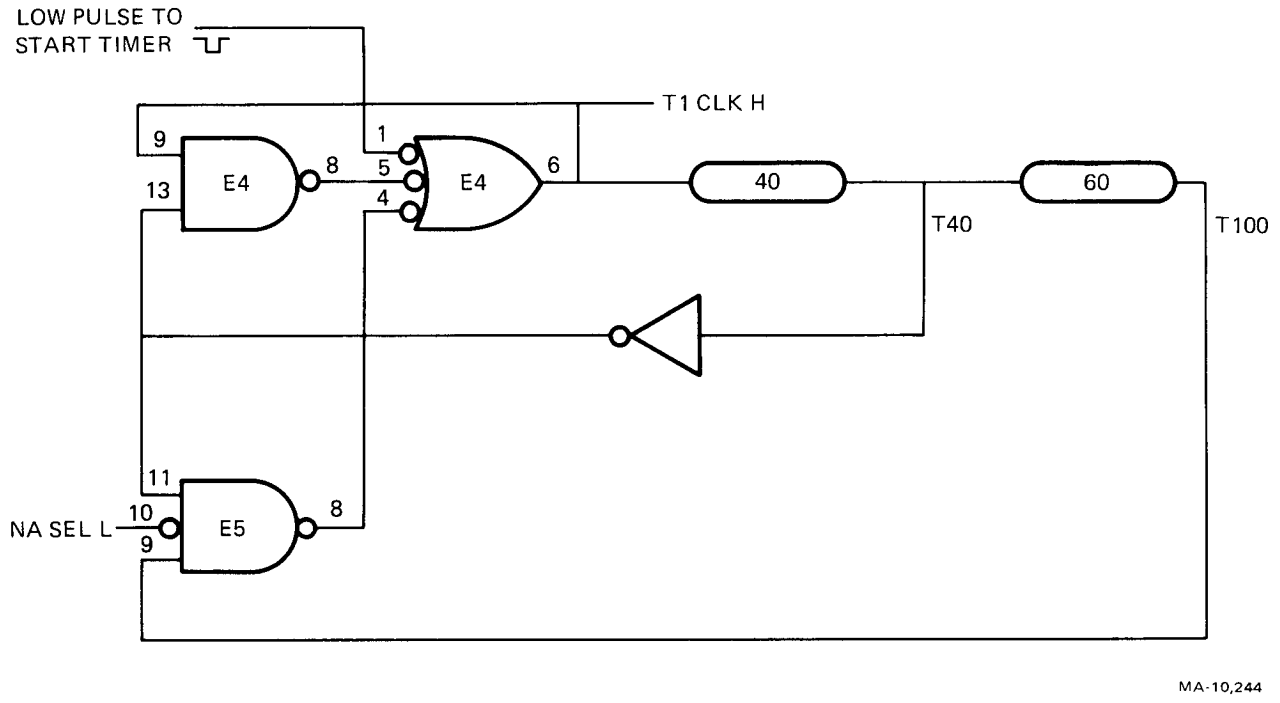


Figure 3-7 Microsequencer Timer Simplified Schematic

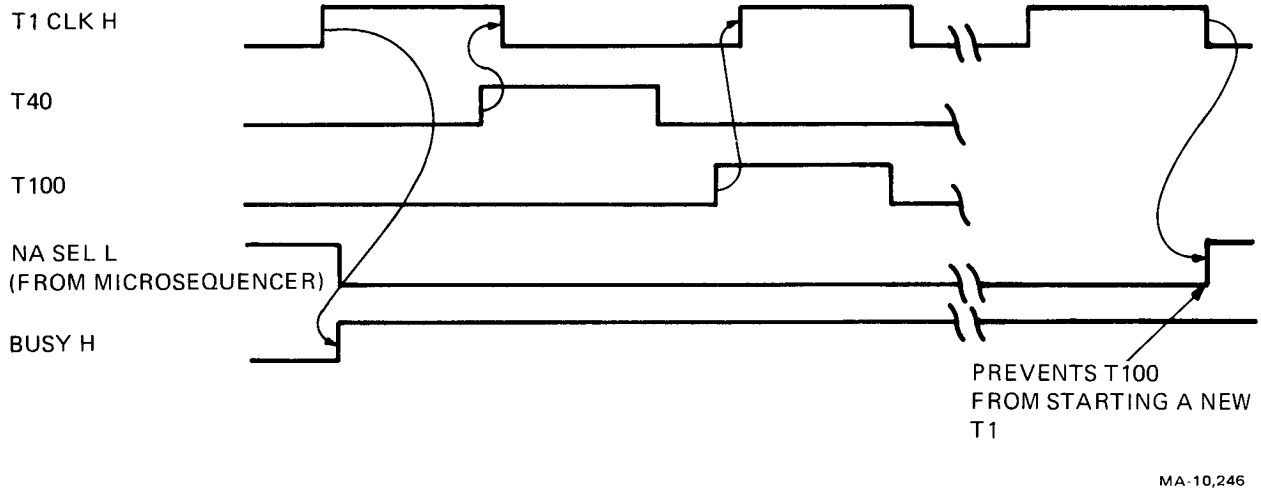


Figure 3-8 Microsequencer Timer Timing Diagram

3.2.6.1 Busy -- Refer to page five of the print set. To prevent interference from other cycle requests, the timer produces BUSY H and BUSY L. BUSY H at E26-12 prevents new requests from disturbing the timer's operation. BUSY is the NOR of the high states of each of delay line output.

The timer's primary output, T1 CLK H, stays high until the high state propagates through the delay line to the 40 ns tap at pin 13. T40 H (E10-13) forces E4-8 high, which forces T1 CLK H low. When T40 H goes high, it also supplies another input to the BUSY NOR gate. This input replaces T1 CLK H, which just went low.

The low signal now propagating through the delay line is 60 ns long, because the next signal that can affect the input signal comes from the 100 ns delay line tap, T100 H (E10-7). Meanwhile, the external latch in the microsequencer circuit needs a clock 60 ns after the start of the cycle. This clock comes from T2 CLK H (E10-5). The BUSY NOR gate uses T40 to fill the 20 ns gap between T1 CLK H and T2 CLK H. Now T2 CLK H stays high for another 40 ns until the signal propagates out T100, and either restarts or stops the timer, depending on NA SEL L. If the timer stops, BUSY L also ends when T2 CLK H goes low. If the timer restarts, BUSY L continues because T1 CLK H goes high.

3.2.7 Diagnostic Decoder

Because the MS11-P memory system is large, a diagnostic program may run in a portion of the same memory array that is being tested. If the memory system is in a diagnostic mode with error correction turned off, errors in the program area of memory can prevent the test program from running correctly. CSR bit 13 specifies that a 16K word portion of memory keep its error protection to protect the test program. CSR bit 3 selects the 16K word portion from the top or bottom half of the first 32K words of the memory system. The diagnostic decoder detects an access to the protected portion of memory, and changes the command inputs to the microsequencer to inhibit diagnostic mode on that access.

Figure 3-9 is a redrawn schematic of the decoder that shows the logic involved. Signals NA 15 H and L indicate whether the address is in the first or second 16K words (refer to Paragraph 3.2.4.3 for details). CSR bit 3 selects which of the NA 15 signals must be asserted to pass through the OR gate. Then the signal is gated by CSR 13 and 1ST 32K HI or LO. If CSR 13 is low then no diagnostic inhibition is wanted. The 1ST 32K signals make sure that inhibition only occurs in the first 128K word portion of memory, although NA 15 reappears for three other segments.

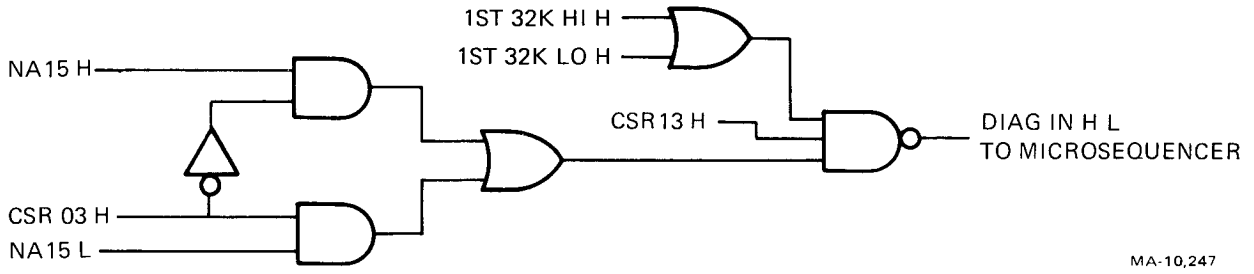


Figure 3-9 Diagnostic Decoder (Redrawn)

3.2.8 Microsequencer

This section describes the microsequencer operation. The control signals it produces that are not related to its operation are described elsewhere in this chapter. The microsequencer is made of four ROMs, a multiplexer, and two latches. Three of the ROMs provide control signals to the rest of the memory system. One ROM and a latch provide addressing for the other ROMs. This addressing controls the actual command sequence. Each ROM has 512 bytes of storage. A memory cycle typically has 5 to 8 steps, and there are 49 combinations of memory cycles and error or diagnostic conditions that need sequences of steps. (Many combinations use the same sequence.) Therefore, each 512 byte ROM has space for control signal data for more conditions than the MS11-P needs.

At the beginning of a memory cycle, the latch E16 outputs are enabled. The latch is supplying an address input to the PROMs. The output of PROM E20 is disabled by NA SEL (next address select) L in the high state. NA SEL L is also the most significant address bit of the four PROMs.

The data at the input of the latch and NA SEL L are the initial address to the microsequencer. For example, if the bus master had requested a DATI cycle, the initial address might appear as shown in Table 3-8.

When the PROMs are clocked by T1 CLK H, the contents of address 14A are available at the PROM outputs (Table 3-9).

The outputs of E25, E29, and E34 are control signals for the other logic on the board. The E20 outputs serve as PROM addresses, which must be set up in time for the next T1 CLK H. The signal NA SEL H is always asserted on the initial T1 CLK H. This is OR'ed with T1 CLK H to create NA SEL L, which serves as a PROM address input, an output enable for latch E16 and E20, and a control signal to the microsequencer timer.

The microsequencer timer, once started, runs until the signal NA SEL L is deasserted. Thus, a DATI cycle to the memory looks like Figure 3-10. The PROM address at T1 CLK H pulse 1 is supplied by the latch and NA SEL L.

Table 3-8 Initial Microsequencer Address

	REF CY H		CSR Ø1 H		ECC INIT L		E16.4	
NA SEL L		DIAG INH L		CSR Ø2 H		C1 H		E163
1	Ø	1	Ø	Ø	1	Ø	1	Ø

1Ø1ØØ1Ø1Ø = 14A in hex notation

Table 3-9 Location 14A Contents

	Hex Location	Hex Data	Binary Data
E2Ø	14A	37	ØØ11Ø111
E25	14A	E3	111ØØØ11
E29	14A	9F	1ØØ11111
E34	14A	A2	1Ø1ØØØ1Ø

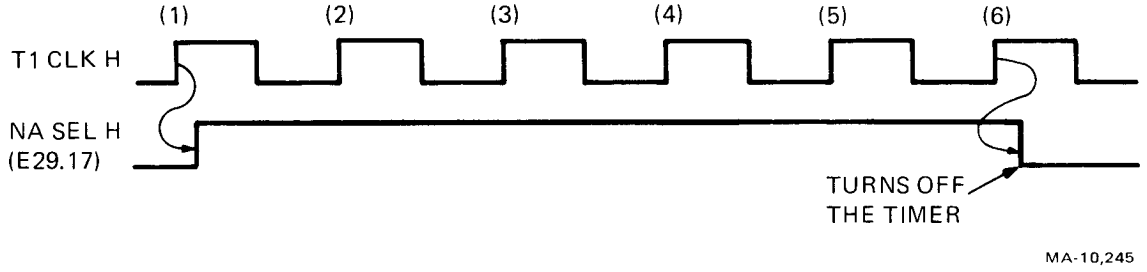


Figure 3-1Ø DATI and Microsequencer Timer

The next PROM address is supplied by the E2Ø outputs. E2Ø's least significant data bits pass through an inverting multiplexer (E2Ø) before becoming PROM address inputs. Therefore, the PROMs see the following address before the second T1 CLK H pulse.

```
Ø           Ø Ø 1 1 Ø 1      Ø Ø = 34 hex
NA SEL L    E2Ø data         Inverted E2Ø data
```

Table 3-1Ø shows PROM data at hex address 34.

The PROMs see the following address before the third T1 CLK H pulse.

```
Ø           Ø Ø 1 1 Ø 1      Ø 1 = 35 hex
NA SEL L    E2Ø data         Inverted E2Ø data
```

Table 3-11 shows PROM data at hex address 35.

The PROMs see the following address before the fourth T1 CLK H pulse.

```
Ø           Ø Ø 1 1 Ø 1      1 Ø = 36 hex
NA SEL L    E2Ø data         Inverted E2Ø data
```

Table 3-12 shows PROM data at hex address 36.

The PROMs see the following address before the fifth T1 CLK H pulse.

```
Ø           Ø Ø 1 1 Ø 1      1 1 = 37 hex
NA SEL L    E2Ø data         Inverted E2Ø data
```

Table 3-13 shows PROM data at hex address 37.

On the fifth T1 CLK H pulse, E29 asserts the signal BR ON E H (branch on error). This signal gates the error flags from the EDC circuitry, through the inverting multiplexer onto the PROM address bus. This is how the microprocessor is informed that an error has occurred. If there are no errors in the data word read from memory (both ERR L and MERR L = high), then E2Ø data passes inverted through the multiplexer. Then the next PROM address is as follows.

```
Ø           Ø Ø 1 1 Ø Ø      Ø Ø = Ø

NA SEL L    E2Ø data         Inverted Error Flags from EDC
```

If a single bit error had occurred and ERR L was asserted low, the PROM would see a different address, and effectively branch to an error handling routine.

Table 3-14 shows PROM data at PROM address Ø.

NA SEL H is now deasserted, which in turn negates NA SEL L, which shuts off the microsequencer timer and ends the cycle.

Table 3-10 Location 34 Contents

	Binary Data
E20	00110110
E25	11100011
E29	10011011
E34	01100010

Table 3-11 Location 35 Contents

	Binary Data
E20	00110101
E25	11100011
E29	10011011
E34	01100010

Table 3-12 Location 36 Contents

	Binary Data
E20	00110100
E25	11101011
E29	10001011
E34	01110010

Table 3-13 Location 37 Contents

	Binary Data
E20	00000011
E25	00100011
E29	11011011
E34	00100010

Table 3-14 Location 0 Contents

	Binary Data
E20	10101010
E25	00100000
E29	00010111
E34	00000000

The PROMs see the following address before the sixth T1 CLK H pulse.

1	1 Ø 1 Ø 1 Ø Ø 1	Ø 1 = 1A9 hex
NA SEL L	E2Ø data	Inverted E2Ø data

Latch E4Ø provides timing delayed from the other control signals. For example, RAS TIM H and CAS TIM H come out of the ROMs in the same T1 clock interval, but CAS TIM H is not needed for another 6Ø nanoseconds. (But, it is needed before the end of the 1ØØ ns T1 clock period). Latch E4Ø gets its inputs from ROM E34 at the same T1 clock as the other signals. However, E4Ø's outputs do not appear until T2 CLK clocks it, 6Ø ns later.

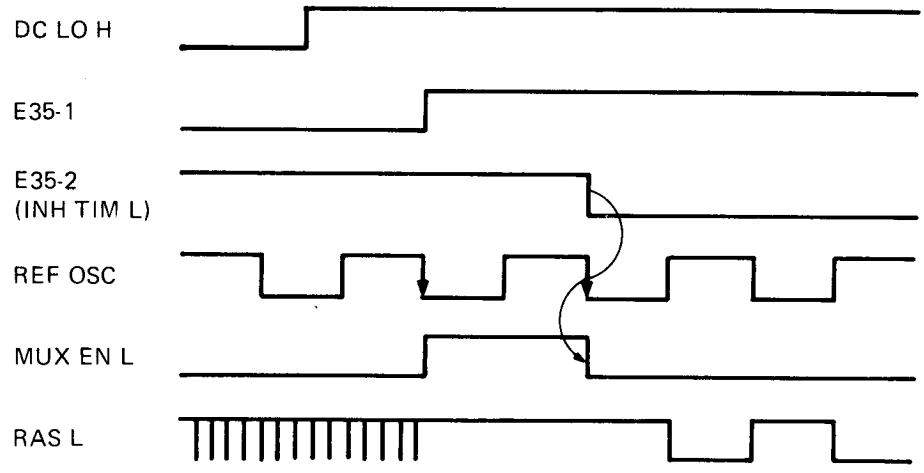
3.2.9 Battery Backup Switch

The central component of the battery backup switch is also the central component of the memory array access control system. E45 is a 4 by 2 multiplexer with inputs from the microsequencer and refresh arbitration logic. Its outputs go to the refresh counter, the array address multiplexers, and the RAS and CAS control logic.

The DC LO detection circuit made of the two flip-flops in E3Ø controls the multiplexer. When power first comes up on both +5 V and +5 VB, BUS DC LO is low and MSØ8 DC LO H is high. The flip-flops power up in unknown states, so the circuit disables all memory array operations until their states are known. Within two refresh oscillator clock periods, the flip-flops are in known states, and memory operations can start.

During normal memory operation, including refresh, the multiplexer's outputs are enabled because MUX EN L (multiplexer enable) is low. While INH TIM L (inhibit time) is high, the multiplexer output signals ROW/COL, SEL/INIT, RAS, and CAS follow inputs from the microsequencer. [ROW/COL controls the array address multiplexers to supply addresses to the RAMs in two steps. SEL/INIT controls the array address multiplexers to provide addressing from the UNIBUS (SEL -- selection) or from the refresh counter (INIT -- initialization and refresh).]

When DC LO goes high, which indicates that +5 V is going down, the memory starts battery backup mode (Figure 3-11). Within one refresh oscillator pulse, MUX EN L goes high, which forces multiplexer E45's outputs high. This prevents the RAS signal from getting to the memory array with glitches, when the array addressing may also have glitches. Within two refresh oscillator pulses, INH TIM L goes low, which forces the microsequencer ROMs to output zeros. This prevents new memory cycles from starting, including normal refreshes. INH TIM L also selects the alternate set of inputs for multiplexer E45. While there are no RAS pulses from E45, there is no refresh. However, the refresh counter does not increment either, so the row that would have been refreshed before MUX EN L went high, gets refreshed only about 15 microseconds later than normal. Then, after some gate delays, MUX EN L goes low, which allows E45's outputs to follow its inputs.



NOTE: INH TIM L GOES TO MUX 2 GATE DELAYS BEFORE MUX EN L RE-ENABLES THE MULTIPLEXOR. NO RAS L DURING MULTIPLEXOR SWITCHOVER TO PREVENT GLITCHES.

MA-10,243

Figure 3-11 Start of Battery Backup Mode

E45 inverts its outputs, so ROW/COL and SEL/INIT go low, CAS goes high, and RAS becomes driven by the refresh oscillator. When both ROW/COL and SEL/INIT are low, they make the array addressing multiplexers select their inputs from the bottom half of the refresh counter. The memories cannot be read or written while CAS is high, so each RAS only refreshes the addressed row in all the RAMs. The RAS signal also clocks the refresh counter, so the next RAS refreshes the next row in the RAMs.

At the end of battery backup mode, when main power comes back up, the timing sequence shown in Figure 3-12 occurs.

3.2.10 Refresh Arbitration

The refresh oscillator's output pulse first passes through a gate that you can disable by grounding DS1 at the backplane. This is a troubleshooting aid, and memory does not use it for its operation. The refresh oscillator output pulse goes to several circuits as a timing source. This section describes the pulse as it is used for refresh only.

If PWR ON L is high, E41 latches the refresh oscillator pulse as REF REQ L (refresh request). REF REQ L goes to latch E41-12 and its inversion goes to E9. E9 passes cycle requests for all memory operations (refer to Figure 3-13, E9 Simplified Schematic). When the microsequencer timer is not busy, the E9 output passes through E2-1 to E41-11 and E3. While E3 delays the timer start, E41 latches REF REQ H as REF CY H (refresh cycle). REF CY H is the refresh cycle request address input to the microsequencer.

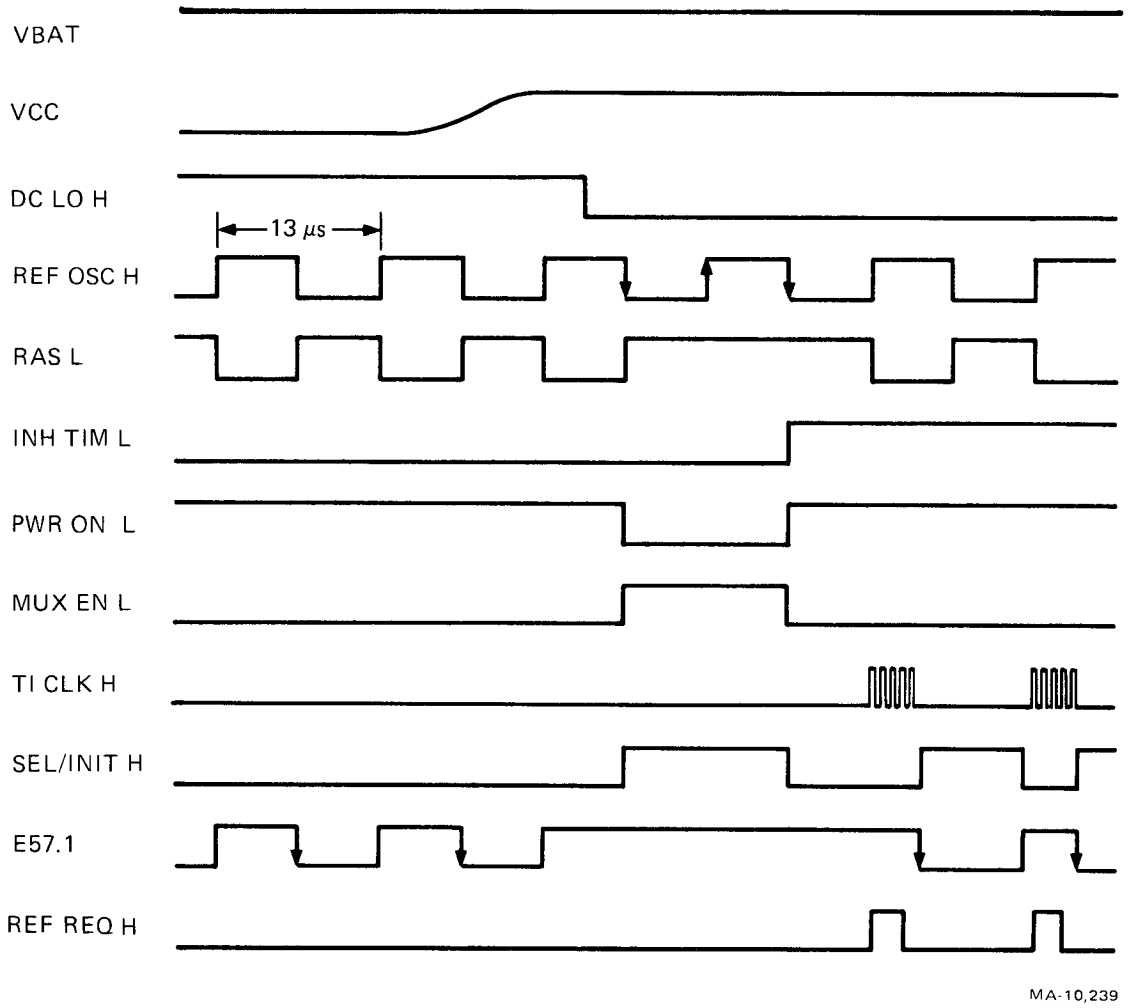


Figure 3-12 End of Battery Backup Mode

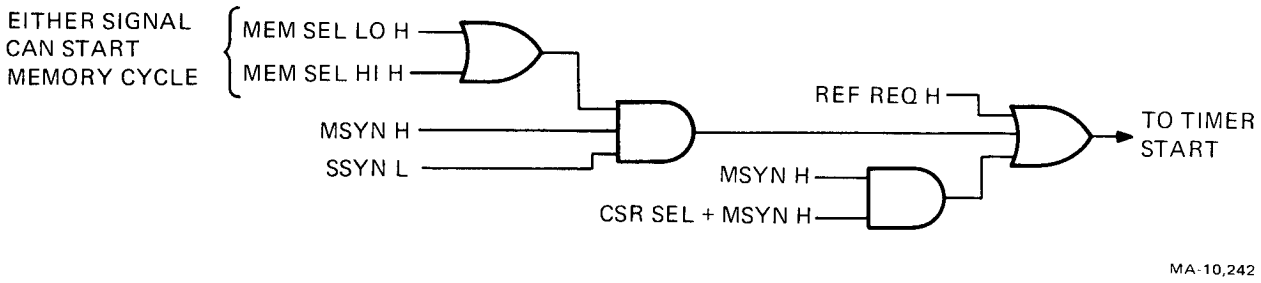


Figure 3-13 E9 Simplified Schematic

When the memory system completes the refresh cycle, the microsequencer outputs the CLR REF H (clear refresh request) signal. CLR REF H resets both latches in E41, which clears the refresh request. The memory system does not perform another refresh cycle until the refresh oscillator outputs another pulse.

3.2.10.1 Microsequencer Timer Hold-off Circuit in Refresh Arbitration Logic -- This circuit delays the timer start until the ROM's address set-up time requirement is met. Most of the microsequencer's address inputs come from relatively slow sources, such as the CSR status outputs and UNIBUS control signals. When these signals are the only ones involved in selecting a timing cycle, the timer can start as soon as all the signals are present.

Both sections of E3 discharge C2 through resistors R2 and R3, and the discrete transistor switch quickly changes state to provide a pulse to the microsequencer timer. However, two kinds of cycles require a slower timer startup.

A refresh request can come at any time. If the system is busy, refresh must wait until the end of the current cycle. The request signals are present at the microsequencer early, but the timer startup request is delayed until the current cycle ends. Therefore, the timer startup delay is not necessary, although it happens anyway. However, if the system is not busy at the time of the refresh request, the request signals appear very quickly at the input to the microsequencer ROM address input, and the timer startup circuit. The timer must be delayed for a few nanoseconds to give the refresh request cycle address time to set up. The bottom half of E3, as shown on page 5 of the schematic, provides the delay time because REF REQ L asserted makes E3-8 high. This prevents discharge through the 18 ohm resistor. Then, the only discharge path for C2 is through E3-6 and a 470 ohm resistor.

CSR accesses are delayed in the same way as refresh requests. This happens because the CSR select signal is used as an address input to the microsequencer, and must be set up in time before the microsequencer is clocked. Finally, if CSR 13 is high, the diagnostic inhibit mode is being used to protect a section of memory. Delay time is added to compensate for the gate delays in the diagnostic address decoder.

CHAPTER 4
MAINTENANCE

4.1 GENERAL

This chapter describes preventive and corrective maintenance procedures that apply to the MS11-P memory. It is an important part of the maintenance philosophy that the user understand normal MS11-P operation as described in the previous chapters. This knowledge, and the maintenance information in this chapter, should enable the user to isolate malfunctions.

Two pieces of equipment are recommended for checking and troubleshooting the memory; a dual-trace 100 MHz oscilloscope and a voltmeter.

You must perform all tests and adjustments in an ambient temperature range of 20` to 30` C (68` to 86` F). Turn off all power (including the battery backup) before you install or remove modules. When the green LED on the MS11-P module is off, it is safe to proceed.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks, performed at intervals, to detect conditions that lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance, and may be performed along with other scheduled preventive maintenance procedures for the computer system.

1. Visual inspection
2. Voltage measurements
3. MAINDEC testing

4.2.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

4.2.2 Power Voltage Check

Once primary power is on, you should check at the backplane the following dc power voltages.

Voltage and Tolerance	Backplane Pin(s)
+5 V ±5%, maximum ripple = Ø.2 V peak-to-peak	AA2, BA2, CA2
+5 VBB ±5%, maximum ripple = Ø.2 V peak-to-peak	BB1, BD1

4.2.3 MAINDEC Testing

You should use the MS11-L/M/P Memory Exerciser (MAINDEC-11-CZMSPA) diagnostic program with the MS11-P memory module. To verify proper operation of the memory, run two passes of the diagnostic. No double errors are permitted. Also, make sure the program printout agrees with the system's total memory.

4.3 CORRECTIVE MAINTENANCE

This paragraph discusses procedures for specific MS11-P corrective maintenance. If you isolate a problem to the MS11-P, you should replace the bad memory with a new memory module, and then retest the system.

You should use the MAINDEC-11-CZMSPA diagnostic for fault isolation (Paragraph 4.2.3). In most cases, you can detect a bad memory module by using the error printout and program listing.

Troubleshooting procedures are presented in the following paragraphs. You can use these procedures in addition to MAINDEC testing, or if you cannot load the diagnostic program. These procedures assume that you already performed a visual inspection and voltage measurements, as specified in Paragraphs 4.2.1 and 4.2.2.

The troubleshooting procedures also assume that the MS11-P starting address is assigned at ØØØØØØ. If any other starting address is used, the operator should modify the following procedures as appropriate.

4.3.1 Initial Check

Load address ØØØØØØ with zeros via the switch register or input device. If you cannot load the proper address (i.e., the proper address is not displayed), check the BUS AC LO L signal at pin BF1 on the backplane. This signal should be high. But if it is not, remove the MS11-P module and check BUS AC LO L again. If the signal at the backplane is now high, the ECC initialize flip-flop (E43) or bus driver (E27) on the board is probably at fault.

If you can load the address, examine the contents of location zero. Then, you should examine the contents of the CSR. If both address zero and the CSR do not respond (i.e., the MS11-P does not return BUS SSYN L), it is likely that a fault exists in E27 (bus driver), E6 (slave sync flip-flop), or the microsequencer, or MSYN H (E54-14) is not reacting properly to BUS MSYN L. The CSR address select logic is probably faulty if address zero only can be accessed; the memory select or timing control logic may be at fault if the CSR only can be accessed.

4.3.2 Refresh Cycle Check

With refresh enabled and the processor halted, the appearance of the REF REQ H pulse (E9-2) at 13 us intervals verifies that the refresh oscillator and refresh request flip-flop are working properly. If REF REQ H is present, check the following signals with an oscilloscope: REF CY H (E16-18), RAS SEL Ø L (E64-3), T1 CLK H (E4-6), CAS A L (E64-18), and CLR REF H (E11-9). The CAS A L signal should be high and the other signals should appear as shown in Figure 4-1. Also check the outputs of the refresh address counter (E51 and E57) to make sure it is incrementing. The failure of any of these signals can result in random loss of data in the MOS storage array.

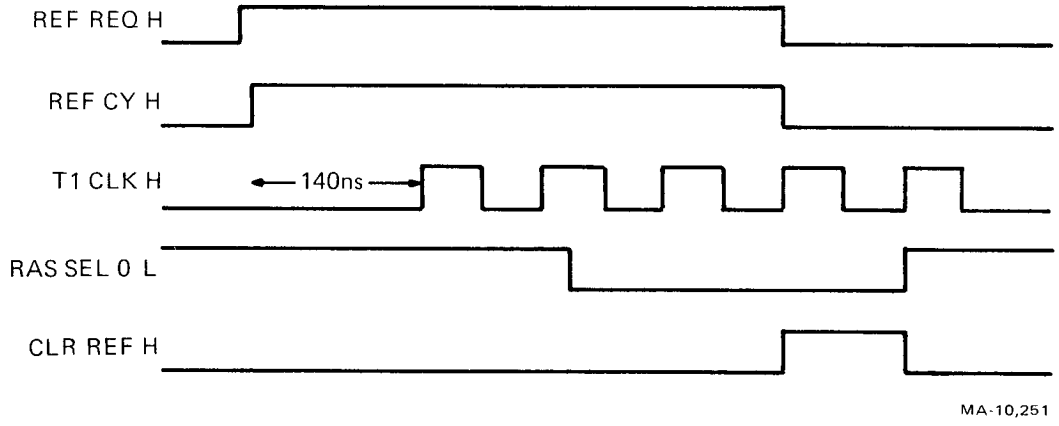


Figure 4-1 Refresh Cycle Check

4.3.3 Read/Write Check

After the memory is initialized successfully, the ECC logic can be checked in the following way.

1. Deposit 1s into locations Ø, 2, 4, 6, 1Ø, and 12. Then examine these locations.

2. Repeat step 1 with Øs if the data is correct. If the examined data in either case is not correct, examine the uncorrectable error flag (bit 15) in the CSR. If it is cleared the ECC logic is probably faulty. If CSR bit 15 is set, disable error correction by setting CSR bit 1. Then deposit/examine as before.

3. If the data is not correct a second time, examine location Ø and then examine CSR bits 15 and 4 (single error flag). With bit 15 set and 4 cleared, there should be a double error within the 22 data bits. With bits 15 and 4 set there should be a single error. If the CSR bits do not agree with the observed error status, the ECC logic is probably bad.

4. Repeat step 3 with locations 2, 4, 6, 1Ø, and 12.

4.3.4 Data Shorts Check

Using memory location ØØØØØØ, check for data line shorts by depositing and examining successively the following data words: ØØØØØ1, ØØØØØ2, ØØØØØ4, ØØØØ1Ø, ØØØØ2Ø, ØØØØ4Ø, ØØØ1ØØ, ØØØ2ØØ, ØØØ4ØØ, ØØ1ØØØ, ØØ2ØØØ, ØØ4ØØØ, Ø1ØØØØ, Ø2ØØØØ, Ø4ØØØØ, 1ØØØØØ. If you do not find any problems, check the address circuitry.

4.3.5 Address Circuits Check (A15 -- AØ1)

To check the address circuits, perform the following procedure.

1. Deposit data word ØØØØØØ in the following locations: ØØØØØØ, ØØØØØ2, ØØØØØ4, ØØØØ1Ø, ØØØØ2Ø, ØØØØ4Ø, ØØØ1ØØ, ØØØ2ØØ, ØØØ4ØØ, ØØ1ØØØ, ØØ2ØØØ, ØØ4ØØØ, Ø1ØØØØ, Ø2ØØØØ, Ø4ØØØØ, 1ØØØØØ.

2. Deposit 777777 in location ØØØØØØ.

3. Examine location ØØØØØ2. The data should be ØØØØØØ as deposited in step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.

4. Deposit 777777 in location ØØØØØ2.

5. Examine location 000004. The data should be 000000, as deposited in step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.

6. Continue the sequence you began in step 2 (for example, location 000004 is next).

4.3.6 Toggle in Memory Test

This test decrements the address, writes 0s, writes 1s, reads 1s, writes 0s, and reads 0s in a given location. It then repeats the above process over a given address range.

Disable the cache if it is enabled. Load 2 into the CSR address to turn off error correction. Load the program starting at address 100000. Set the top address to 100000 and the bottom address to 0. This checks memory over the first 16K. If this test is successful, load the program starting at address 0. Set the top address to 177776. Set the bottom address to 100000. This checks memory over the second 16K, where the absolute loader will reside.

R0 = Highest address
R1 = Lowest address

```
 0      012700                  MOV # top address, R0
 2      Top address
 4      012701                  MOV # bottom address, R1
 6      Bottom address
10      005040          A:      CLR - (R0)
12      005110                  COM (R0)
14      022710                  CMP #177777, (R0)
16      177777
20      001007                  BNE B
22      005110                  COM (R0)
24      22710                   CMP #0, (R0)
26      0
30      001003                  BNE B
32      020001                  CMP R0, R1
34      001365                  BNE A
36      000000                  HALT;               ;test complete
40      000000          B:      HALT;               ;error
```

If no error is found, the program stops with the PC pointing to location 40. If an error occurs, the program stops with the PC pointing to location 42, and the failing address is contained in R0.

NOTE

To check the second 16K bank, make sure that memory management is enabled, and the appropriate relocation constants are specified. (Refer to the PDP-11/44 CP Subsystem Technical Manual, EK-KD11Z-TM.)

4.3.7 Diagnostic Check Mode Usage

Bit 2 (diagnostic check mode) allows check bits in the MOS storage array to be read via the CSR. Right after a DATI bus cycle to memory (with bit 2 equal to 1), the CSR should be read with a DATI cycle to examine check bits retrieved from the storage array. Note that a DATO cycle to the CSR destroys the retrieved check bits, but an error address recorded in the CSR is preserved.

The diagnostic check mode also provides a way to test the error correction logic by allowing the check bit pattern in a 22-bit word to be altered via the CSR. The desired check bit pattern should be written into CSR bits 10 -- 5 and bit 2 should be set to 1 with a DATO cycle to the CSR. A DATO cycle to memory should then be performed. Writing the appropriate check bit pattern in the storage array should cause the detection and correction of a single-bit error during a subsequent memory read cycle.

For example, the check bit pattern, generated on a data pattern of all 0s, is 001100. If the user alters the check bit pattern to 000010, the ECC logic should change data bit 0 in the 22-bit word from 0 to 1. To implement this example, the user should write 000010 into CSR bits 10 -- 5, and 1 into CSR bit 2, with a DATO bus cycle. The user should then perform several DATO cycles to memory by writing zeros into several consecutive locations. And, CSR bit 2 should be cleared to zero. When the user reads the same memory locations with DATI cycles, the least significant bit of each location written should contain a one.

4.3.8 Clearing a Double Error

ECC initialization clears memory by writing zeros and appropriate check bits into all memory locations. To implement initialization, turn off system power and the battery backup unit (if present). Then, power up the system to start initialization. Note that knowledge of the double-error location is not required; however, all data in memory is also erased.

To specify the error correction disable mode, write a logical one into CSR bit 1 with a DATO cycle. Then, write the correct data into the appropriate memory location(s) to clear the double error. Writing a zero into CSR bit one then enables error correction for normal operation.

APPENDIX A
GLOSSARY AND NOTES

GLOSSARY

This glossary explains the signal names that appear in the Field Maintenance Print Set timing diagrams. The names appear here in the same order that they appear in the timing diagrams.

DATI Cycle

MSYN	Master sync from the bus master at the bus receiver output.
T1 CLK	100 nanosecond period clock from microsequencer timer.
T2 CLK	100 nanosecond period clock delayed by 60 ns from microsequencer timer.
BUSY	Indicator that microsequencer timer is running.
NA SEL	Next address select, from microsequencer, also combined with T1 CLK. Most significant bit of microsequencer cycle address.
RAM X A1 -- A8	Outputs of RAM array addressing multiplexers. Crossover shows where change from row to column addressing occurs.
RAS TIM	Output from microsequencer that times RAS for complete memory system. Goes through battery backup multiplexer on page MS05.
RAS SEL 0 -- 7	Decoded bank selection on page MS04. RAM array is addressed directly with 16 bits to select one of 64K. Another four bits select one of eight 64K banks to supply with RAS.
R/C TIM	Row/column time -- output from microsequencer that times change from row to column addressing for complete memory system. Goes through battery backup multiplexer on page MS05.

CAS TIM	Output from microsequencer that times CAS for complete memory system. Goes through battery backup multiplexer on page MSØ5.
CAS A -- D	Outputs of array CAS drivers.
D15 -- DØØ	Shows time when data from RAMs becomes stable on internal data bus.
BR ON E	Branch on Error -- signal from microsequencer that switches inputs on multiplexer E21 (page MSØ6) and enables microsequencer to branch to an error handling routine if error correction and detection circuit (EDC) found error in read data.
LE IN	Latch enable in -- EDC control signal from microsequencer. Loads data and check bit input latches.
LE OUT	Latch enable out -- EDC control signal from microsequencer. Enables data output latches according to OE BYTE.
OE BYTE Ø,1	Output enable byte Ø,1 -- two signals from microsequencer to EDC that select byte zero, byte one, or both, for output.
CLK SSYN	Clock slave sync -- output from microsequencer that starts SSYN propagating through gates to appear on bus at right time. If there is an error, ERR L at E6 on page MSØ6 prevents SSYN until error is corrected, and SSYN is set directly by SET SSYN from microsequencer.
BUS SSYN	Time that slave sync appears on UNIBUS to indicate that data is available.
EN DEC	Enable decode -- CSR control output from microsequencer, starts CSR cycle by decoding command inputs CC, CB, CA. Signal is delayed in latch E4Ø to allow setup time for CSR.
CC,CB,CA	CSR command inputs from microsequencer.

Additional Signals for DATO Cycle

WE TIM	Write enable time -- output from microsequencer that times writing for complete memory system.
WE A -- D	Outputs of array write enable drivers.

BYT Ø,1 EN	Byte Ø,1 enable -- outputs from microsequencer that select bytes from data bus to be loaded into EDC for checkbit generation and writing to memory.
GENERATE	Output from microsequencer that tells EDC that data is stable so it can generate checkbits.
OE SC	Output enable syndromes or checkbits -- puts checkbits on data bus for writing to RAMs.
SET SSYN	Output from microsequencer that causes BUS SSYN. SSYN indicates to bus master that memory system has accepted data from UNIBUS.

Additional Signal for DATI, CSR

PASSTHRU	Output from microsequencer that lets data through EDC without being modified.

Additional Signals for Refresh Cycle

REF OSC	Refresh oscillator -- continuously runs with 12.5 microsecond period.
REF REQ	Refresh request -- REF OSC is latched if power is normal.
REF CY	Refresh cycle -- output from refresh arbitration logic.
SEL/INIT	Select/initialize -- output from battery backup multiplexer that selects memory access addressing (location selection) or initialization addressing.
ROW/COL	Row/column -- output from battery backup multiplexer that selects addressing for RAMs.
RAS	Output from battery backup multiplexer that supplies RAS timing to memory system.
E57.1	Clock input to refresh counter.
CLR REF	Clear refresh -- output from microsequencer that clears latched REF REF and REF CY at end of refresh cycle.

PRINT SET NOTES

On page MSØ5, the two flip-flops in E41 have "6Ø NS" printed next to them. This indicates that E41 is a special part that is guaranteed to recover from a possible race condition, within that amount of time. Such a condition can happen if a memory access request arrives at exactly the same time that the refresh oscillator requests a refresh cycle. This problem only affects the half of E41 clocked at pin 11.

Vertical bars that cross signal lines at many places in the prints have a special meaning. The drawing system used to design the MS11-P uses that symbol to indicate apparent mismatches between signal assertion levels (as suggested by their names) and the logic input assertion levels that the signals are connected to.

APPENDIX B
HANDLING ELECTROSTATIC SENSITIVE DEVICES

HANDLING PROCEDURES

You can handle static-sensitive devices with reduced risk once the devices are soldered into modules. To keep the risk at nearly zero, it is necessary to handle, store, and ship the modules in anti-static containers. You can keep the risk acceptably low by taking the following precautions.

1. Unpack and install finished modules at grounded work stations.

2. If a grounded work station is not available, handle a module either by its top or edges, away from the components and gold fingers on the edges. Or, preferably they should be contained in approved anti-static bags or boxes.

3. Ship modules bare in cardboard cartons.

4. If plastic shipping material is used (foam, plastic bags, or bubble pack,) make sure it is anti-static, or treated with anti-static liquid.

5. In areas where operators stay in one place, the operator is kept at ground potential with a conductive wrist strap connected to a ground through a 250-kilohm resistor. The bench top is also connected to ground.

SUPPLIES

There are Digital Equipment Corporation part numbers and approved sources for some anti-static and electrostatic discharge (ESD) control supplies. You must use existing corporate parts, sources, and procedures. The individual that requests the parts, material, or equipment is responsible for complying with this requirement. The Module Process Handbook, A-MN-ELMF308-0-0 provides more information.